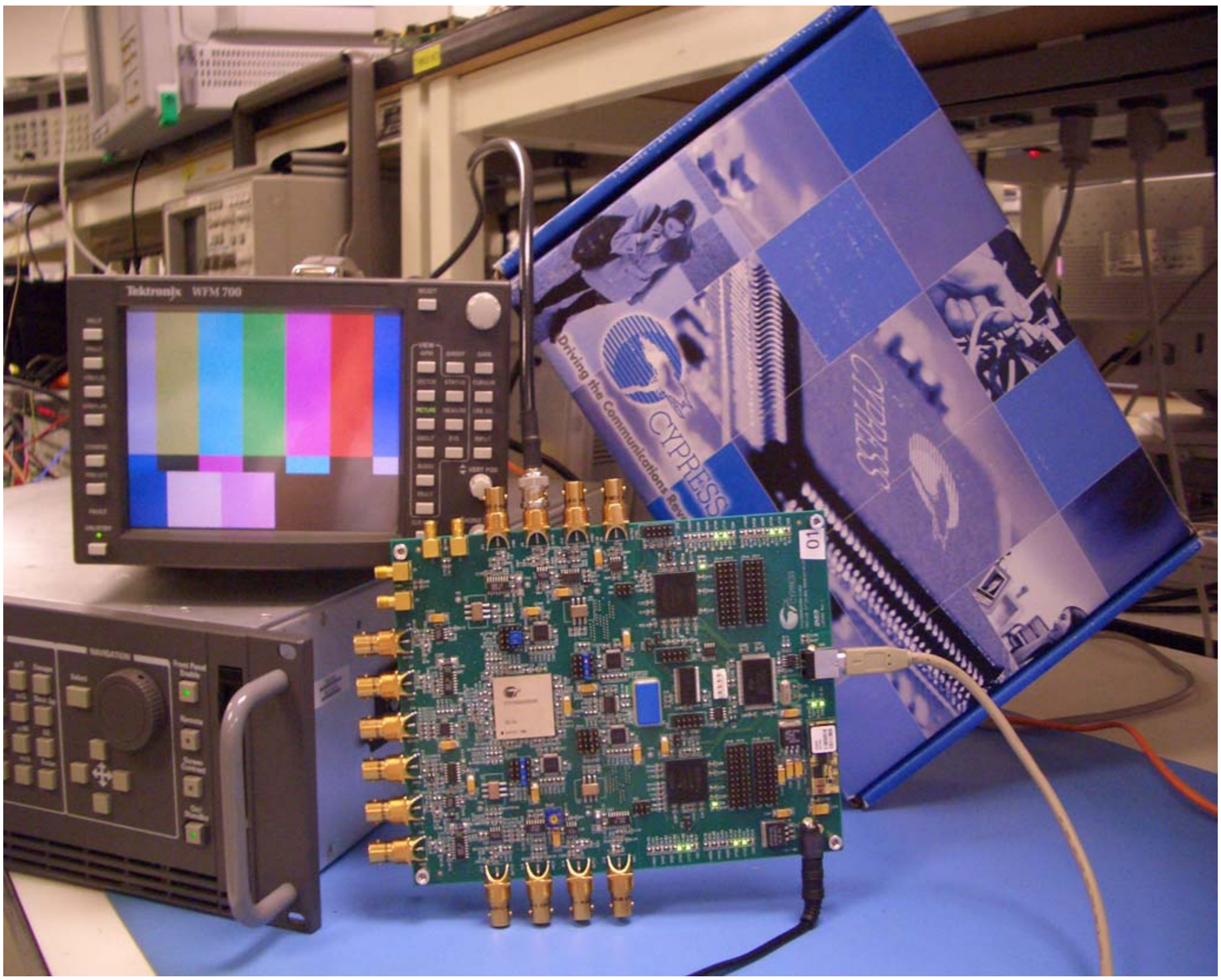
Quad Independent Channel HOTLink II™ CYV15G0404DXB Video PHY Demonstration Board Users Guide



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1.0 Introduction

The Quad Independent Channel HOTLink II™ CYV15G0404DXB Video Demonstration (Demo) Board is a full-fledged serial digital video reference platform that demonstrates the HOTLink II video physical layers (PHYs) interfacing to industry-standard cable drivers and equalizers. Upstream processing of the video data is performed using on-board Altera Cyclone FPGAs. The board also has a flexible clocking architecture with automatic rate detection that allows the board to pass video traffic in multiple formats.

The Independent Channel HOTLink II devices[1] are capable of simultaneously operating each channel at a different data rate. The CYV15G0404DXB has the additional capability of performing independent reclocking on a per-channel basis.

The Independent Channel HOTLink II CYV15G0404DXB Video Demo Board demonstrates:

- the ability of the Cypress family of transceivers to pass serial digital video at signaling rates from 270 Mb/s to 1485 Mb/s
- the independent channel functionality of the applicable devices[1]
- the ability to use a HOTLink II transceiver with an FPGA for auto rate detection and clock reconfiguration
- the ability to perform reclocking in the HOTLink II CYV15G0404DXB device
- the flexible configuration abilities of Cypress Microsystems' PSoC™ microcontroller
- the use of Cypress EZ-USB FX2™ USB microcontroller for video data and in-system configuration applications
- on-board FPGAs that generate and receive different video test patterns.

Although this board uses the CYV15G0404DXB device, the same board can be used as an evaluation vehicle for any device in the HOTLink II Independent Channel family of devices. Please refer to the data sheets for descriptions of the HOTLink II Independent Channel family of devices.

2.0 Kit Contents

The kit contains the following:

1. Quad Independent Channel HOTLink II CYV15G0404DXB Video PHY Demo Board, as shown in *Figure 2-1.*
2. CD containing:
   a. Graphical User Interface (GUI) set-up file[2]
   b. Application Notes
   c. Demo board user's guide (this document)
   d. Cypress' device data sheets
   e. Schematics
3. 75Ω Coaxial cable
4. AC/DC wall adapter
5. USB cable
6. *Dear Customer* Letter
7. Kit checklist.

Notes:
1. The Independent Channel HOTLink II family consists of the CYV15G0403DXB, CYV15G0404DXB, CYV15G0104TRB, CYV15G0203TB, CYV15G0204RB, CYV15G0204TRB, CYV15G0403TB, CYV15G0404RB. Refer to each data sheet for a description.
2. Please see Appendix E for instructions on installation.

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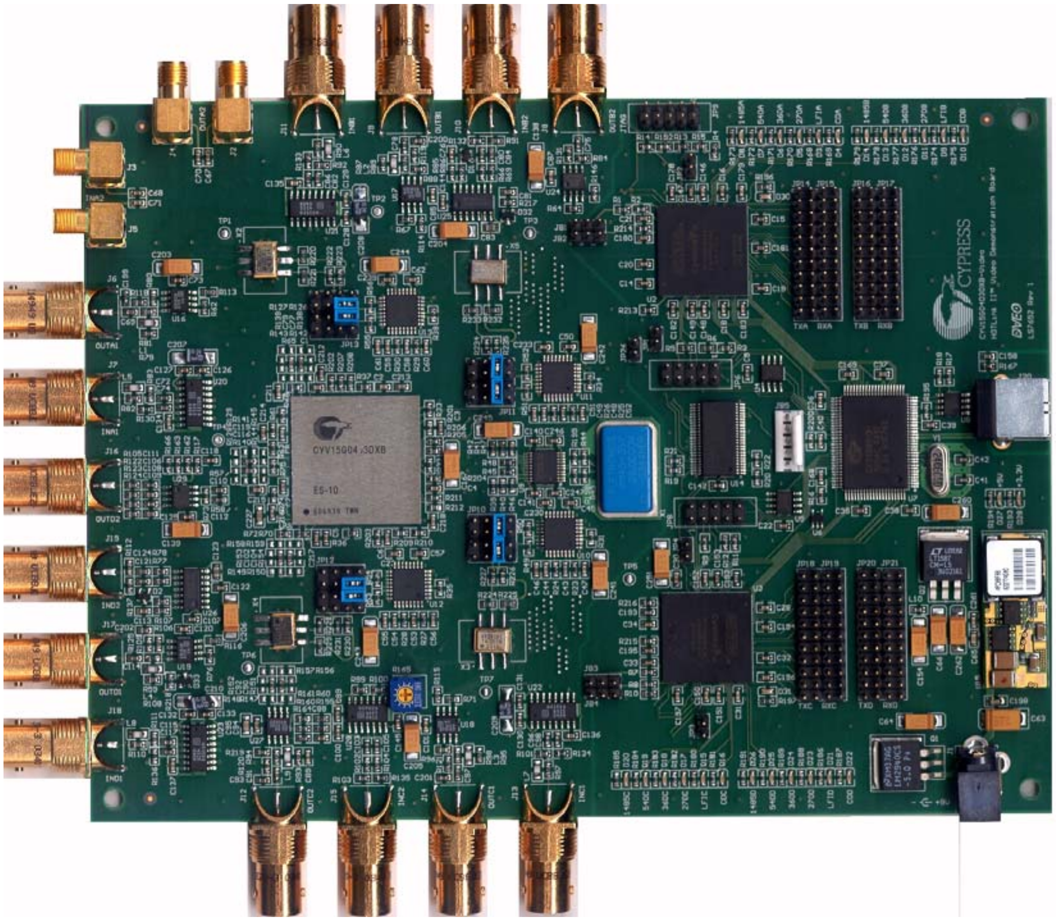


Figure 2-1. Top View of Video Demo Board

3.0 Demo Board Features

This section highlights the key features of the Quad Independent Channel HOTLink II CYV15G0404DXB Video PHY Demo Board.

- Video transport at multiple rates of 270 Mb/s, 360 Mb/s, 540 Mb/s, and 1485 Mb/s
- Auto-rate detection
- Low-Jitter outputs
- Programmable clocking options for different SMPTE data rates
- SMPTE scrambler/descrambler functionality implemented in FPGA
- 4x4 clock header to support multiple clocking options
- High-speed USB FX2 microcontroller to configure FPGAs
- Configuration of HOTLink II device using Cypress Microsystems PSoC™ Microcontroller
- Reclocking Deserializers
- 6V DC supply with on-board voltage regulator to prevent noise transfer from external power sources
- Interfaces to industry-standard equalizers and cable drivers
- LED status indicators
- User-friendly GUI
- Windows® 2000/XP supported.

4.0 Board Architecture

The architecture of the board is shown in *Figure 4-1* through *Figure 4-4*.

The heart of the board is the Quad Independent Channel HOTLink II CYV15G0404DXB device. The device has four independent transceiver channels. Each transceiver has a transmitter with two outputs and a receiver with two selectable inputs. Each CYV15G0404DXB channel also incorporates a reclocking deserializer. Each transmitter performs 10-to-1 serialization. Each receiver includes a Clock and Data Recovery PLL (CDR PLL with embedded VCO and loop filter) and 1-to-10 deserializer. On the board, the parallel interface of the CYV15G0404DXB is connected to the on-board FPGAs (U2 and U3). All serial outputs (except OUTA2) are connected to commercially-available cable drivers. All serial inputs (excluding INA2) are connected to commercially-available equalizers. The CYV15G0404DXB is configured via an 8-bit data/4-bit address configuration interface. This configuration is controlled via a Cypress Microsystems PSoC microcontroller (U14). The architecture of the board is described in the following sections.

4.1 Cable Driver and Equalizer Interfaces

The serial I/Os of the HOTLink II device are connected to various equalizers on the receive side and various cable drivers on the transmit side as shown in *Figure 4-1*. The different cable drivers, equalizers and their connections to the HOTLink II device are shown in *Table 4-1*. Note that all primary interfaces (INx1 and OUTx1) of each channel support multiformat (both HD and SD) drivers and equalizers, while the secondary interfaces (INx2 and OUTx2) support SD only.

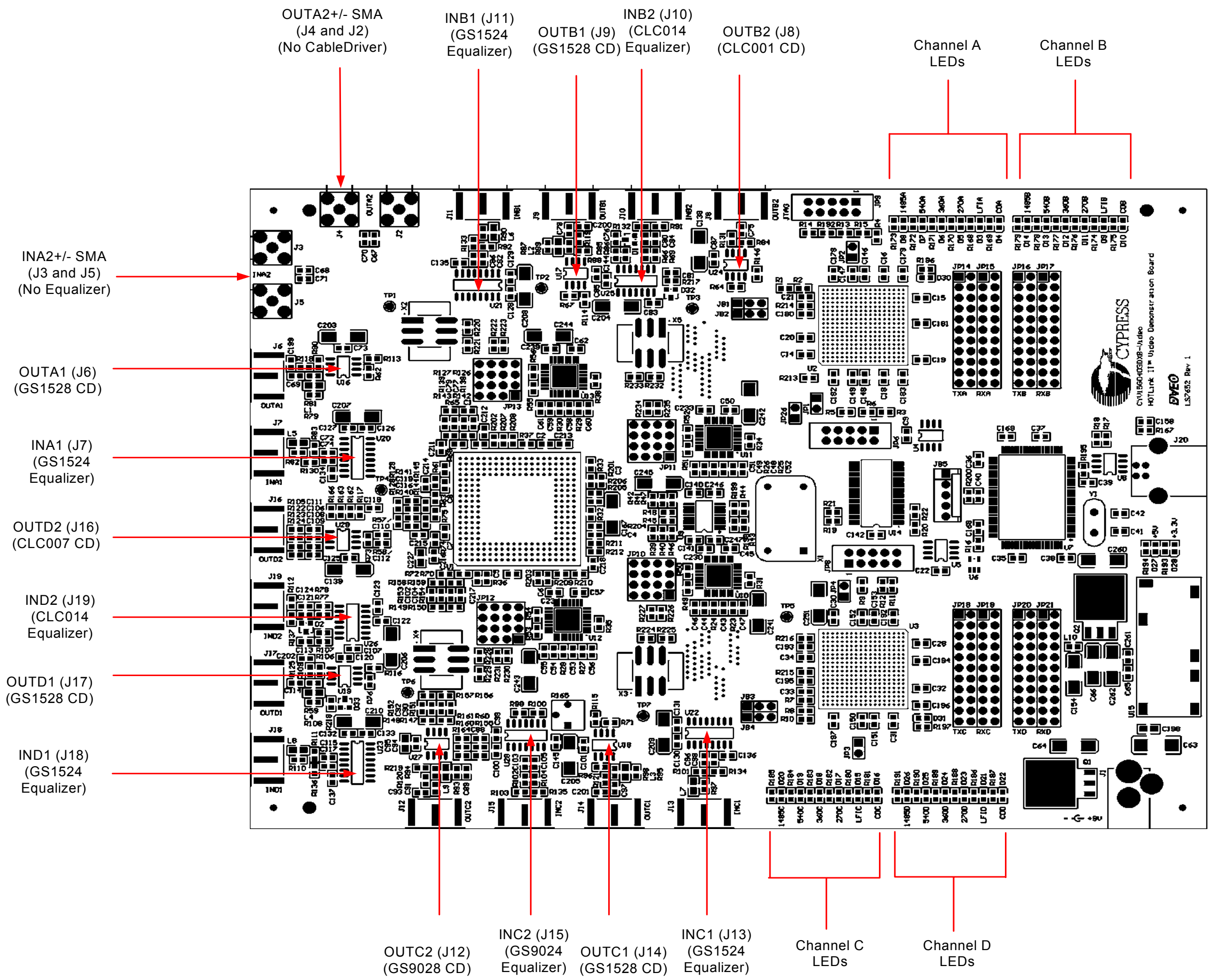


Figure 4-1. Placement of Cable Drivers and Equalizers and Channel-specific LEDs

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Table 4-1. Interface of Cable Drivers and Equalizers to HOTLink II Serial I/Os

HOTLink II Channel	Serial I/O of HOTLink II Device	Interfacing Cable Driver	Interfacing Equalizer	Supported Standard
Channel A	OUTA1±	Gennum GS1528	x	HD-SDI and SD-SDI
	INA1±	x	Gennum GS1524	
	OUTA2±	No Cable Driver (SMA)	x	Supports any data rate from 195 Mb/s–1500 Mb/s (not SMPTE-compliant)
	INA2±	x	No Equalizer (SMA)	
Channel B	OUTB1±	Gennum GS1528	x	HD-SDI and SD-SDI
	INB1±	x	Gennum GS1524	
	OUTB2±	National CLC001	x	SD-SDI
	INB2±	x	National CLC014	
Channel C	OUTC1±	Gennum GS1528	x	HD-SDI and SD-SDI
	INC1±	x	Gennum GS1524	
	OUTC2±	Gennum GS9028	x	SD-SDI
	INC2±	x	Gennum GS9024	
Channel D	OUTD1±	Gennum GS1528	x	HD-SDI and SD-SDI
	IND1±	x	Gennum GS1524	
	OUTD2±	National CLC007	x	SD-SDI
	IND2±	x	National CLC014	

4.2 Clocking Architecture

The board has multiple clocking options to allow for flexible testing and configuration. On each channel, the user can select either the on-board programmable clock, on-board 74.25-MHz crystal oscillator (for HD-SDI/SMPTE 292M), a clock provided by the FPGA, or an external clock. The on-board programmable clock plays a useful role in the auto rate detection mechanism, which dynamically reprograms the reference clock to the correct frequency, based on the incoming SDI data rate.

When transmitting the video test patterns generated by the FPGA, either the programmable clock, external clock or on-board crystal oscillator (only for HD-SDI) should be used.

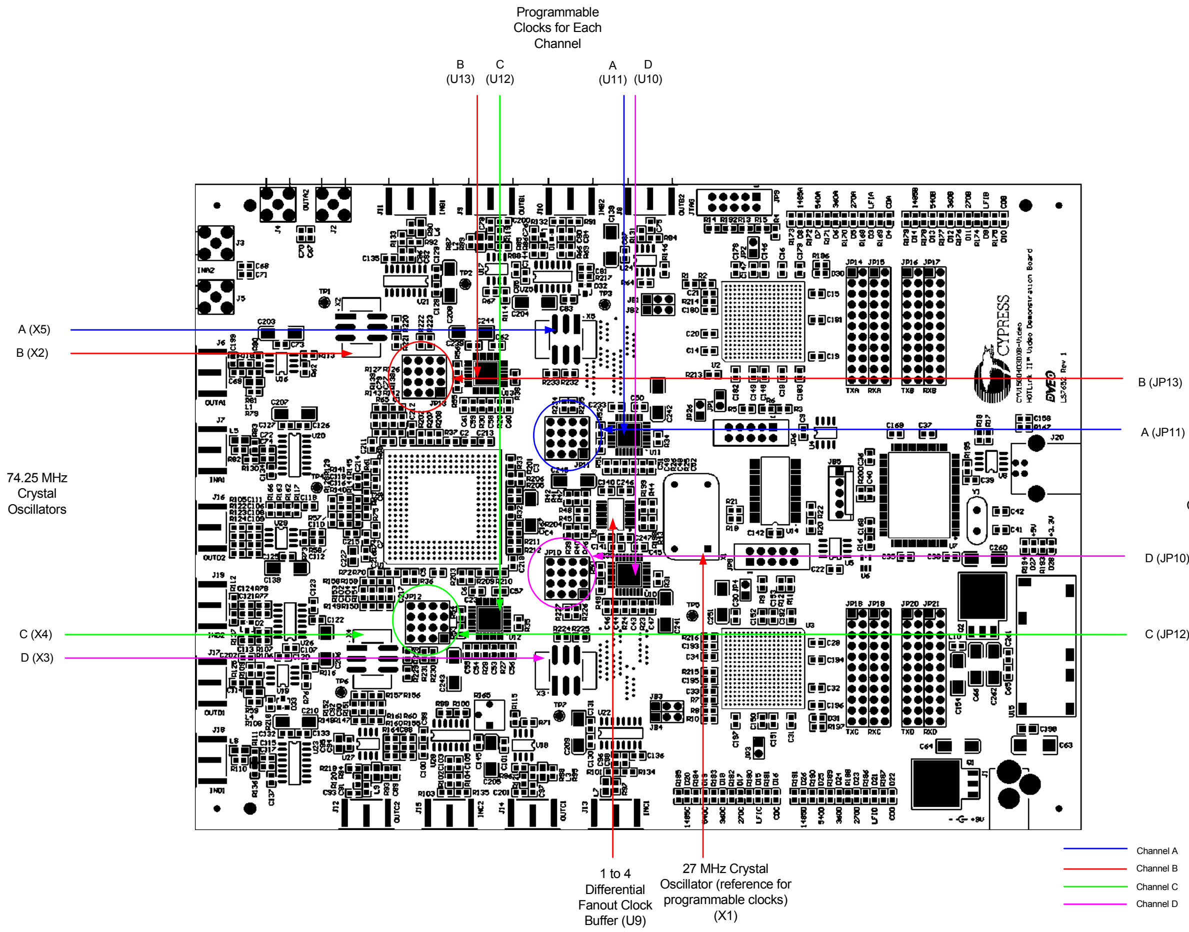


Figure 4-2. Placement of Clocks on the Board

Note. For HD-SDI transmit jitter measurements, it is recommended to avoid using the programmable clock due to the high intrinsic jitter generated by this clock. This jitter will not influence the output jitter in reclocker mode, so the programmable clock may be used to measure reclocked jitter generation. To measure HD-SDI transmit jitter of the HOTLink II video demo board, it is recommended to use the on-board crystal oscillator.

The board allows various video test patterns to be generated by the FPGA at different rates and transmitted through serial outputs. The selection of the pattern and data rate is made through the USB host interface GUI. Clock configuration instructions are given in *Figure 4-3*.

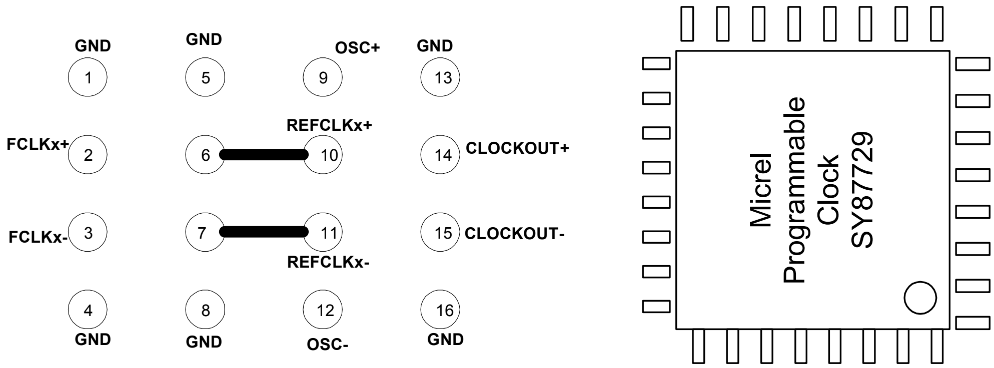
If the programmable clock option is selected, the data rate setting in the GUI controls the output frequency of the programmable clock. If the external clock option is selected, the user must ensure that the external clock frequency matches the data rate setting in the GUI. For HD-SDI, either a full-rate (148.5 MHz or 148.5/1.001 MHz) or half-rate (74.25 MHz or 74.25/1.001 MHz) clock may be used. If the on-board 74.25-MHz crystal oscillator option is selected, the GUI must be set to 1485 Mb/s and the FR (Full-Rate) box should be left unchecked.

For further details on jitter measurement, please see application note entitled, *SDI SMPTE Jitter Performance of the Independent Channel HOTLink II™ Transceiver*.

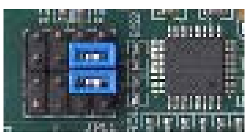
Configuration instructions for the different clocking options are found in *Figure 4-3*.

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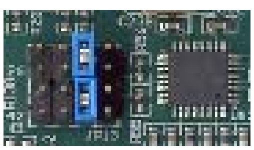
JP10, JP11, JP12, JP13



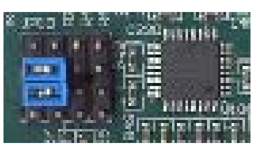
The position of the Micrel programmable clock chip is given to set the correct orientation for determining the pin numbers for clock configuration. Note: Jumpers 6 and 10, and jumpers 7 and 11 are physically shorted for header design considerations.



On board programmable clock option:
Jumper 14 to 10 and Jumper 15 to 11 for using Programmable Micrel clock as Reference Clock. Remove all other jumpers from the header. This option must be chosen if the auto rate detect feature of the board is used.



On board 74.25 MHz crystal oscillator clock option:
Jumper 9 to 10 and Jumper 12 to 11 for using 74.25 MHz crystal oscillator clock as Reference Clock. All other jumpers must be removed. This option should be chosen for HD-SDI transmit jitter measurement. The GUI must be set to a datarate of 1485 Mb/s (FR box unchecked) for the associated channel.



FPGA clock option:
Jumper 2 to 6 and Jumper 3 to 7 for using FPGA clock (FCLK) as Reference Clock. Remove all other jumpers from the clock configuration header. This clock option is only used when implementing the upconversion feature of the board. See Appendix F for further details.

External clock option:
Remove all jumpers from the clock configuration header. Provide a differential clock to pins 6 and 7, with pins 5 and 8 as respective grounds (pins 6 and 5 and pins 7 and 8 are signal and ground pairs). Ensure that the GUI is set to the same clock frequency as the external clock.

Figure 4-3. Clock Configuration

4.3 FPGA and Control Architecture

The board contains two FPGAs, U2 and U3. The FPGA U2 interfaces to channels A and B of the CYV15G0404DXB device. The FPGA U3 interfaces to channels C and D of the CYV15G0404DXB device. The major functions performed by the FPGA are as follows.

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1. Video test pattern generation. For SD-SDI, the FPGA can generate EG1 Color Bar Data, Grey Pattern, SMPTE RP178, and SMPTE RP178 alternate SDI checkfield patterns. For HD-SDI, the FPGA can generate Color Bar Data, Grey Pattern, SMPTE RP198, and SMPTE RP198 alternate SDI checkfield patterns.
2. Auto rate detection and clock reconfiguration. The FPGA plays an important role in automatically detecting the incoming data rate and reconfiguring the programmable clock to the correct frequency.

The CYV15G0404DXB configuration interface (8-bit data and 4-bit address) is configured through a Cypress Microsystems PSoC microcontroller. The PSoC receives instructions from the host PC through the on-board USB interface.

The on-board USB interface is used to control the various operating modes of the device through a flexible GUI. The USB interface is also used to re-program the FPGA and the PSoC microcontroller.

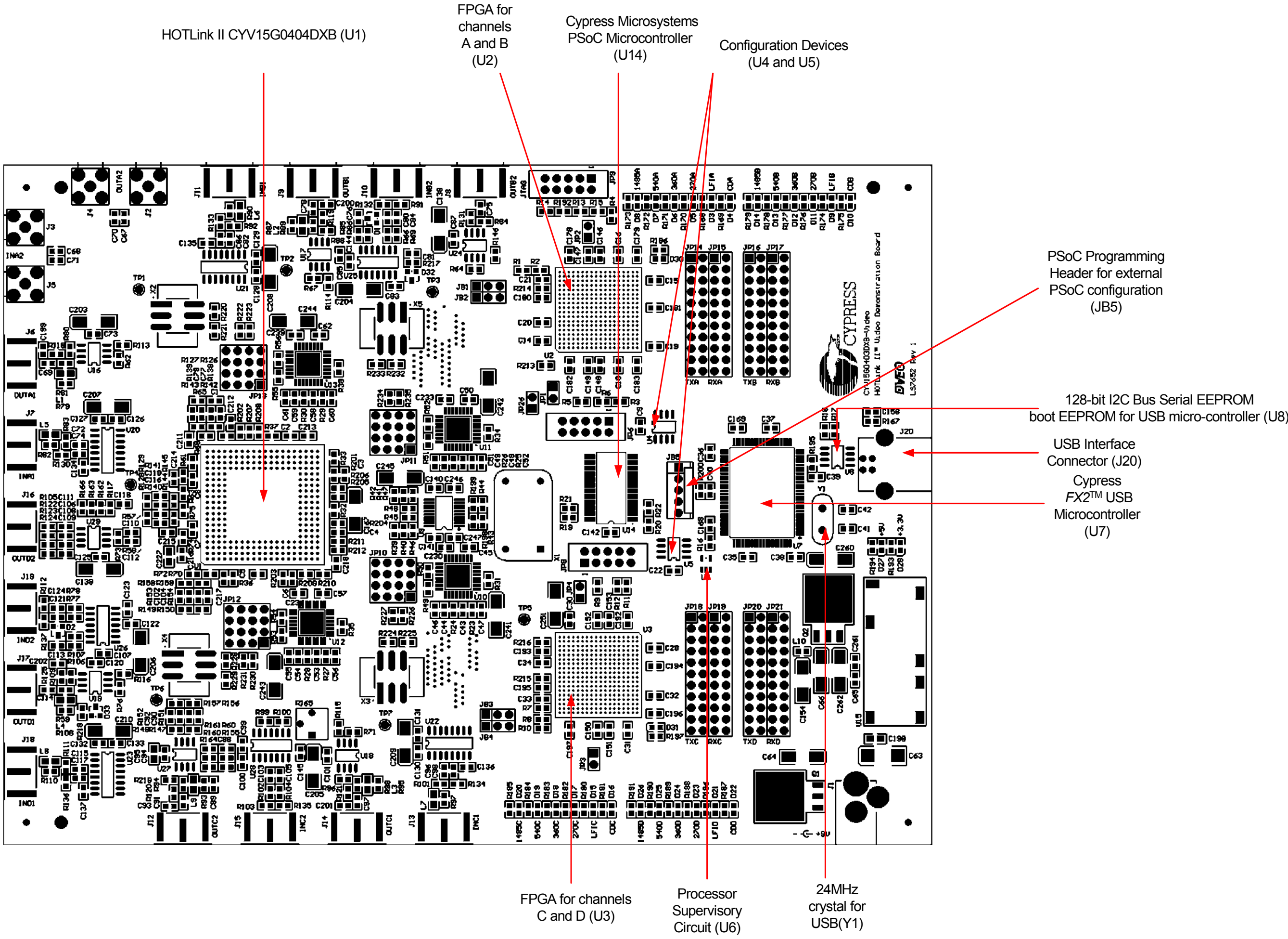


Figure 4-4. Placement of FPGA and Controls

4.4 Power Supply

The entire board is powered through a single 6V DC power supply. The 6V input is down-converted using on-board regulators to different voltages for the various devices in the board. The kit for the board includes a compatible 6V AC wall power supply adapter.

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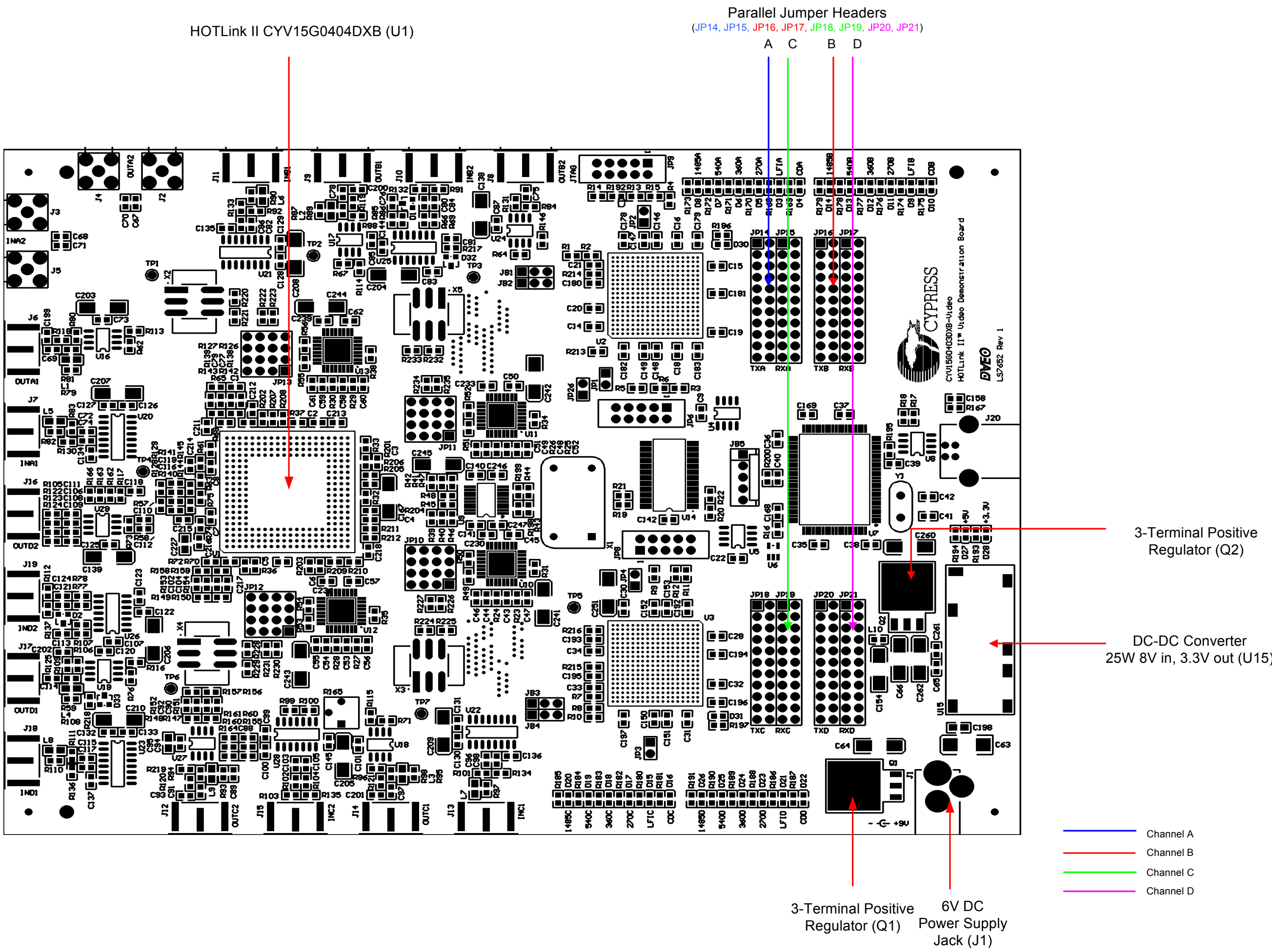


Figure 4-5. Placement of Power Supply and Jumper Headers

5.0 GUI and Operating Modes

Please refer to Appendix E for instructions on installing the GUI on a PC/Laptop and configuring the computer to recognize the USB device. A picture of the GUI window is presented in *Figure 5-1*. A summary of the functionality of the buttons for channel A is presented in *Table 5-1*. The description of each button's functionality applies equally to all channels.

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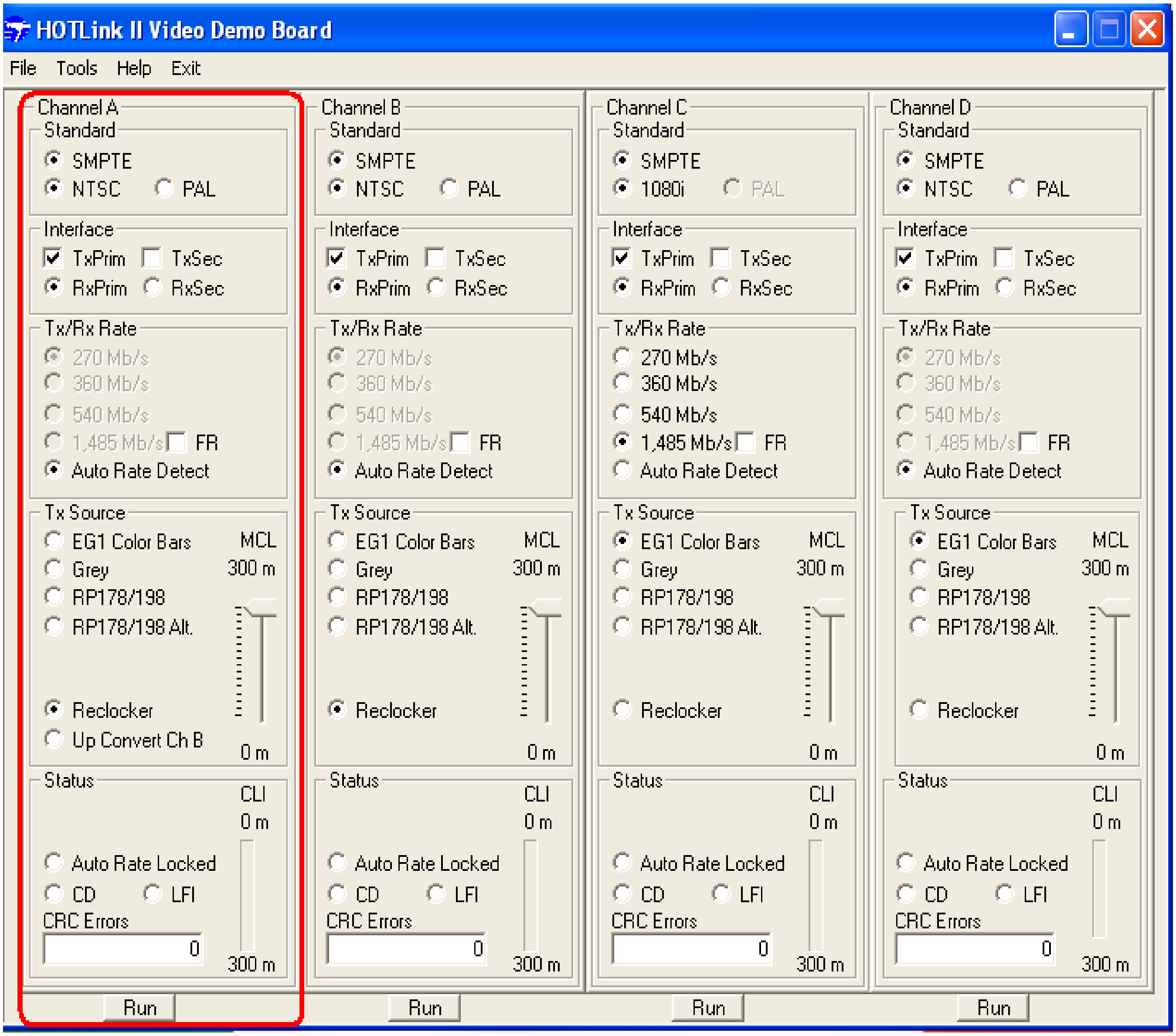


Figure 5-1. Graphical User Interface

Table 5-1. Summary of GUI Button Functionality (Shown Here for Channel A)

Group	Button Name	Functionality (On Click)
Standard	SMPTE	No action. This radio button is always selected.
	1080i (see channel C in the above figure)	Standard for HD-SDI, automatically checked when user selects 1485Mb/s in Tx/Rx Rate Panel of the GUI.
	NTSC	Standard for SD-SDI. The user can check NTSC when they are transmitting/receiving data at 270 Mb/s, 360 Mb/s, or 540 Mb/s.
	PAL	Standard for SD-SDI. The user can check PAL when they are transmitting/receiving data at 270 Mb/s, 360 Mb/s, or 540 Mb/s.
Interface	TxPrim	Transmit data via OUTA1 (supports both SD and HD)
	TxSec	Transmit data via OUTA2 (supports SD only)
	RxPrim	Receive data via INA1 (supports both SD and HD)

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Table 5-1. Summary of GUI Button Functionality (Shown Here for Channel A) (continued)

Group	Button Name	Functionality (On Click)
	RxSec	Receive data via INA2 (supports SD only)
Tx/Rx Rate	270 Mb/s	SD-SDI: SMPTE 259M-C
	360 Mb/s	SD-SDI: SMPTE 259M-D
	540 Mb/s	SD-SDI: SMPTE 344M
	1485 Mb/s	HD-SDI: SMPTE 292M
	Auto Rate Detect	Programmable clock is reconfigured to the incoming video data rate and all other Tx/Rx Rate buttons will display which frequency the programmable clock is set to.
	FR	Setting the source clock frequency for HD-SDI as either full-rate (148.5 MHz) or half rate (74.25 MHz). When the check-box is checked, a full-rate 148.5 MHz clock is used; when unchecked, a 74.25 MHz clock is used.
Tx Source	EG1 Color Bars	The FPGA generates EG1 color bars, which will be transmitted out on OUTA1 or OUTA2 or both.
	Grey	The FPGA generates a uniform grey pattern, which will be transmitted out on OUTA1 or OUTA2 or both.
	RP178/198	The FPGA generates RP178/198 pattern (a pink half-frame on top of a grey half-frame, which will be transmitted out on OUTA1 or OUTA2 or both.
	RP 178/198 Alt.	The FPGA generates an alternative set of the RP178/198 pattern which will be transmitted out on OUTA1 or OUTA2 or both.
	Reclocker	Reclock the recovered data from the clock and data recovery unit and retransmit it through the serial outputs of the same channel.
	Up Convert Ch B	Functionality not yet implemented.
	MCL	Maximum Cable Length: for normal operation there is no need for the user to touch this (i.e. leave at 300m). If user would like to test at specific cable lengths then the bar can be set to the desired setting.
Status	Auto Rate Locked	Button selected when the correct data rate is detected.
	CD	Carrier Detect: Button selected when the amplitude of the signal on equalizer is above the MCL threshold.
	LFI	Link Fault Indicator: Button automatically selected when HOTLink II CYV15G0404DXB does NOT receive a valid serial signal on the relevant channel.
	CRC Errors	Cyclic Redundancy Check Errors Indicator Bar: indicator bar indicates data reception errors.
	CLI	Cable Length Indicator: estimates length of the cable being used for transmitting/receiving data. Output from cable equalizer.
Channel A	Run/Stop	Hitting run configures the channel with the applied settings; hitting stop ends operation and powers down channel A.

5.1 Setting the SDI Data Rate

The appropriate data rate is set by selecting the appropriate button in the Tx/Rx Rate Box of the GUI. The various data rate options are 270 Mb/s (SD-SDI/SMPTE 259M-C), 360 Mb/s (SMPTE 259M-D), 540 Mb/s (SMPTE 344M) or 1485 Mb/s (HD-SDI). See *Figure 5-2* for a picture of this GUI panel. The FR (Full Rate) check box adjacent to the 1485-Mb/s option is for setting the source clock frequency for HD-SDI as either full-rate (148.5 MHz) or half-rate (74.25 MHz), via the programmable clock. When the check-box is checked, a full-rate 148.5-MHz clock is used, and when unchecked, a 74.25-MHz clock is used. This button is active only when the 1485-Mb/s button is selected.

If the programmable clock option is selected, the data rate setting in the GUI controls the output frequency of the programmable clock. If the external clock option is selected, the user must ensure that the external clock frequency matches the data rate setting in the GUI. If the on-board 74.25-MHz crystal oscillator is used, the 1485 Mb/s option must be selected with the FR box left unchecked. See Section 4.2 for information on selecting clock options.

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If the output is to be viewed on a Tektronix WFM 700 waveform monitor, the user should not select the 360 Mb/s or 540 Mb/s options because this waveform monitor does not support these data rates, and consequently, no images will be displayed on the monitor.

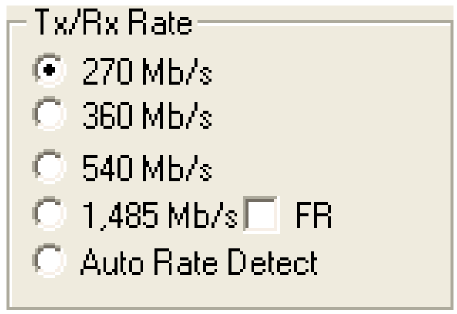


Figure 5-2. GUI–Setting the Data Rate

Auto Rate Detect

When the Auto Rate Detect button is selected, the programmable clock is reconfigured to match the incoming video data rate and all other data rate buttons will be disabled. Upon clicking "Run," various rates are attempted until a valid SMPTE data rate is detected on the input. This is shown as the last button in *Figure 5-2*. During the Auto Rate Detection function, a radial dot loops through each data rate as it is attempted. If the data rate is successfully detected, the dot stops next to the rate of the incoming data stream. For this feature to function, the programmable clock option must be selected.

5.2 Serial Interface I/O Selection

Each HOTLink II transmit channel has redundant outputs. Either one or both outputs can be enabled to transmit the same data. When TxPrim is checked, the primary serial outputs OUTx1 are enabled. When TxSec is checked, the secondary serial outputs OUTx2 are enabled. Note that both primary and secondary outputs can be enabled simultaneously. Each HOTLink II receive channel has selectable dual inputs. Either INx1 (RxPrim) or INx2(RxSec), but not both, can be selected as the input serial data source for the respective channel. See *Figure 5-3* for a picture of the GUI panel.

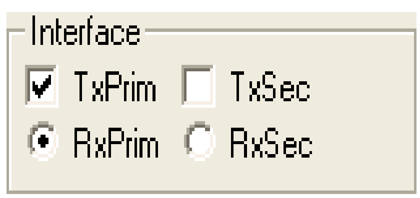


Figure 5-3. GUI–Selecting the Serial I/Os

5.3 Standard

The first box in the top of the GUI sets the video standard. For SD, the supported SMPTE formats are NTSC and PAL as shown in *Figure 5-4*. For HD, the supported format is 1080i and upon selecting 1485 Mb/s in the "Tx/Rx Rate" panel, the "Standard" panel will reflect the HD standard as shown in *Figure 5-5*.



Figure 5-4. GUI–Selecting the Standards–SD

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Figure 5-5. GUI–Selecting the Standards–HD

5.4 Transmit Test Pattern

For SD-SDI, the FPGA can be configured to generate EG1 Color Bar, SMPTE RP178 SDI checkfield, SMPTE RP178 Alternate SDI checkfield, or Grey field patterns. For HD-SDI, the FPGA can be configured to generate Color Bar, SMPTE RP198 SDI checkfield, SMPTE RP198 Alternate SDI checkfield, or Grey field patterns. The Maximum Cable Length (MCL) scroll bar should be set to 300m for normal operating conditions. See *Figure 5-6* for details.

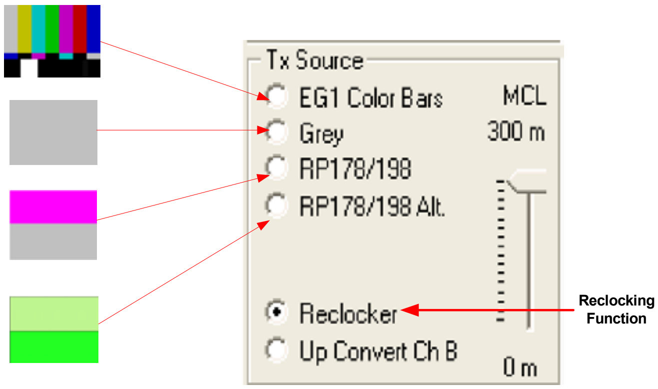


Figure 5-6. GUI–Selecting the Test Patterns

Reclocker

The CYV15G0404DXB has an integrated reclocker function to reclock the recovered data from the clock and data recovery unit and retransmit it through the serial outputs of the same channel. This can be set by selecting the Reclocker button. If both Reclocker and Auto Rate Detect are selected, and the programmable clocking option is enabled, the auto rate detect logic will detect the incoming data rate and reconfigure the clocks to perform reclocking function on the selected channel. See *Figure 5-6* for a picture of the reclocker radio button.

5.5 Status

The status panel reflects the real time status of the board; the user has no control of this panel. The “Cable Length Indicator (CLI)” estimates the length of the cable being used between a transmitter and the receiver on that channel. The “Cyclic Redundancy Check (CRC) Errors” status bar indicates the number of errors detected after the received signal goes through the appropriate cyclic redundancy check. The “Link Fault Indicator (LFI)” is asserted when the HOTLink II CYV15G0404DXB does not receive a valid signal. The “Carrier Detect (CD)” is automatically checked when the amplitude of the incoming signal is greater than the threshold. The “Auto Rate Locked” button is selected when the data rate for incoming data is detected and the clock is programmed to the corresponding frequency.

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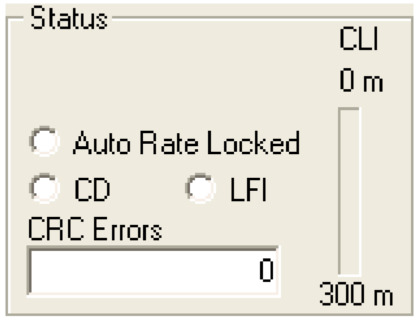


Figure 5-7. GUI–Selecting Status

6.0 Sample Test Procedures

Before performing the sample tests, please be sure to read Appendix E. It contains instructions on installing the GUI and configuring the hardware completely. Note: The on-board FPGAs and PSoC will be preprogrammed at the factory for testing. Therefore there should be no need to program them. Appendix E contains programming instructions should you need them.

6.1 Required Equipment

- Tektronix Waveform Monitor: WFM 700
- Quad Independent Channel HOTLink II CYV15G0404DXB Video PHY Demo Board
- PC/Laptop with HVDB installed
- USB cable
- 6V DC Power Supply
- Four–six BNC cables

6.2 Tektronix WFM 700

The Tektronix WFM 700 is used in the demo tests to display the signal(s) output by the video demo board on the channel(s) specified by the user. As mentioned in previous sections, the WFM 700 does not support data rates of 360 Mb/s and 540 Mb/s. For a brief description of relevant buttons for the tests, please see *Figure 6-1*. The connectors used in the tests are shown in *Figure 6-2*.

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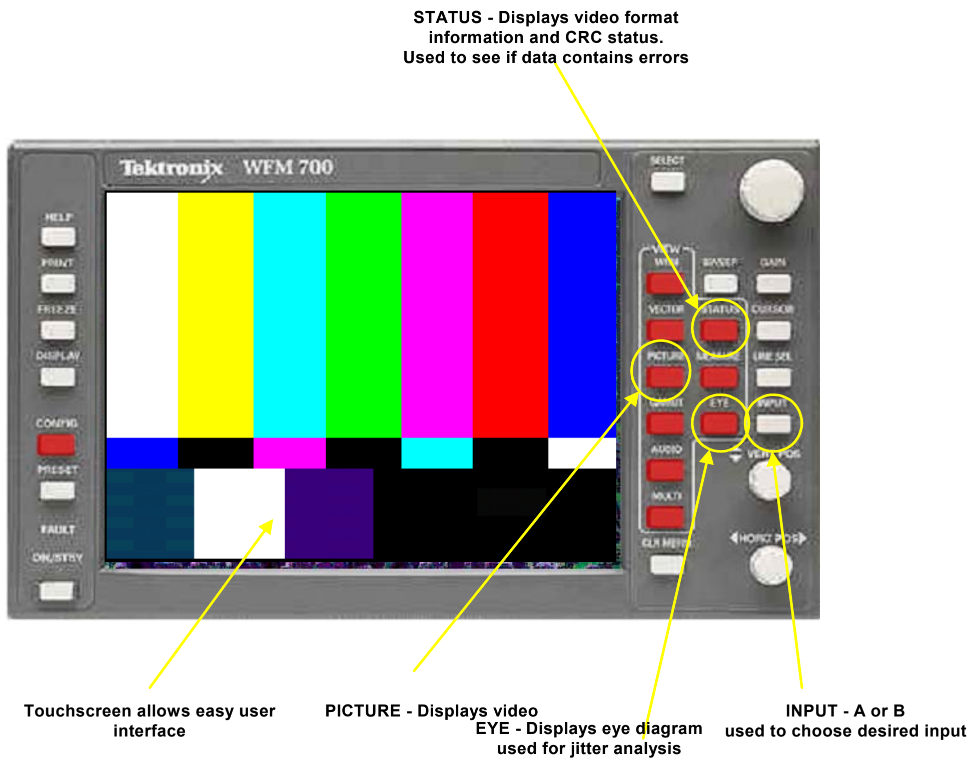


Figure 6-1. Tektronix WFM 700–Front View

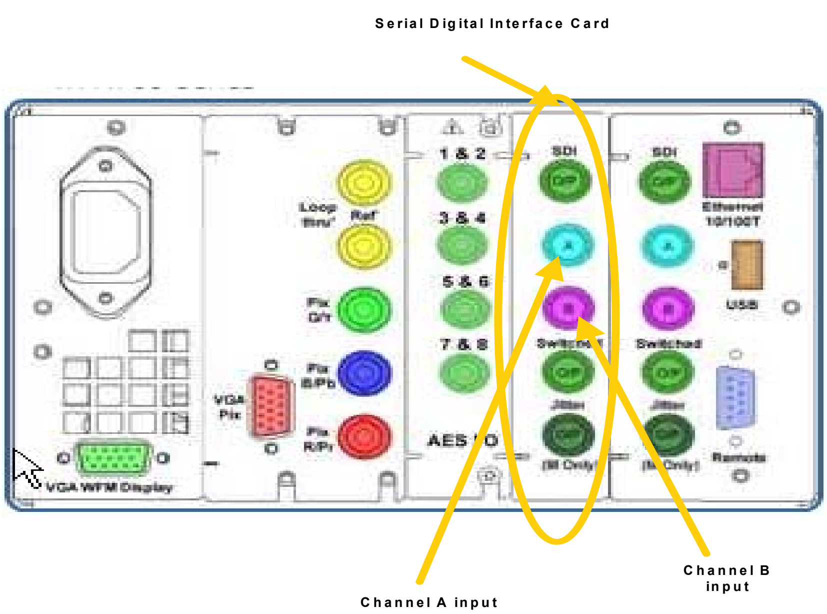


Figure 6-2. Tektronix WFM 700–Rear View

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6.3 Tests

This section contains step-by-step tests for fully evaluating the functionality of the board.

6.3.1 Generating SD Color Bar Patterns

1. Apply power to the board and connect the USB cable between the board and the computer.
2. Connect output OUTA1 to input A of the WFM700 using a BNC cable.
3. Open the GUI.
4. Configure channel A to generate color bars in SD format. In the “Tx/Rx Rate” panel of the GUI, click on the radio box for 270 Mb/s. In the “Tx Source” panel, select “EG1 Color Bars” to generate the color bar in SD format. See *Figure 6-4* for the GUI setting for transmitting color bar at 270 Mb/s.
5. Select the programmable clocking option as shown in *Figure 4-3*.
6. Press the “Run” button for channel A.
7. View the picture and status displays for the signal on the WFM 700.

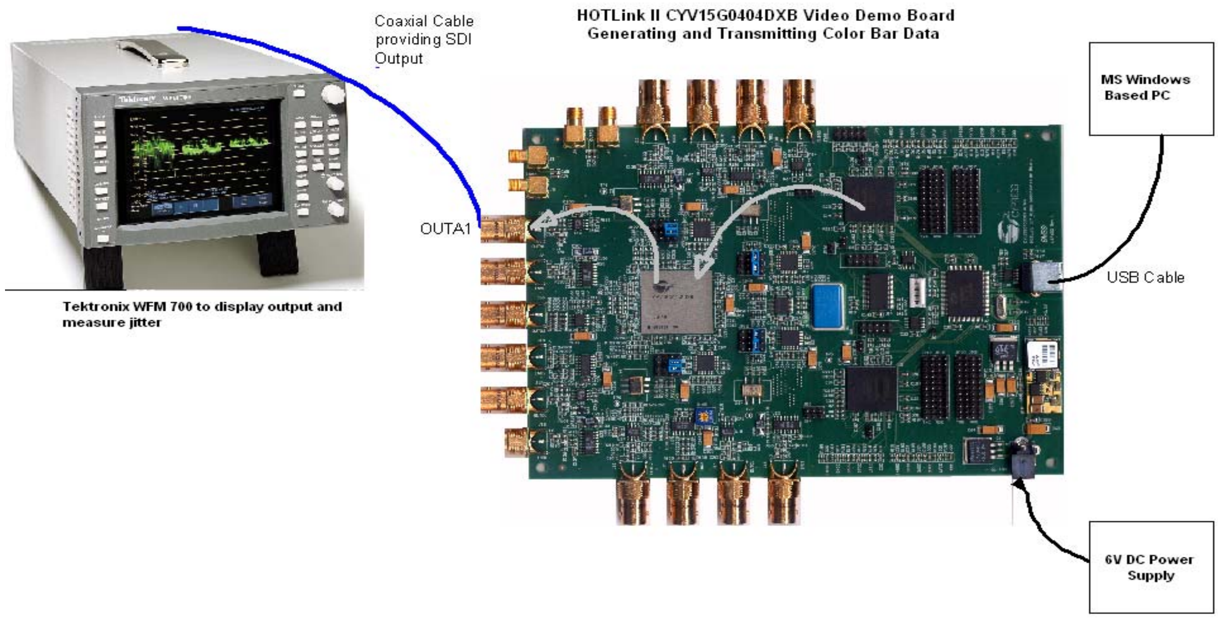


Figure 6-3. Sample Test 1–Generating and Transmitting Color Bars

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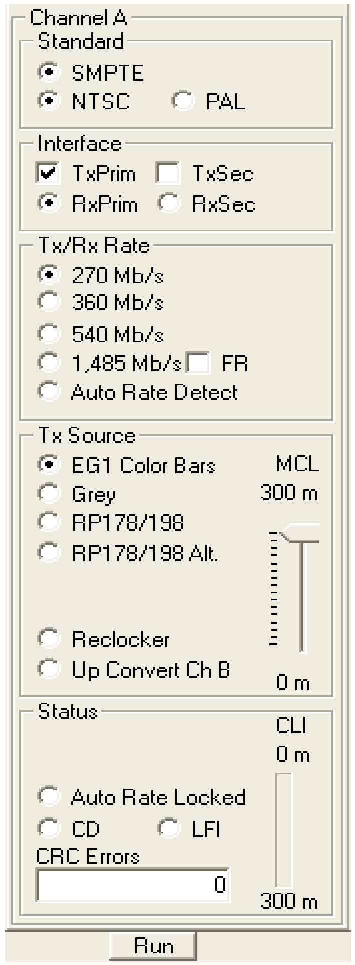


Figure 6-4. GUI Setting for Sample Test 1

6.3.2 Generating HD Color Bar Patterns and Reclocking the Data Three Times

1. Apply power to the board and connect the USB cable between the board and the computer.
2. Connect a BNC cable between OUTC1 and IND1, a cable between OUTD1 and INB1, a cable between OUTB1 and INA1, and a cable from OUTA1 to WFM 700. The pattern is sent from the FPGA to channel C; the data is then reclocked from channel C to channel D, then reclocked from channel D to channel B, then reclocked from channel B to channel A and then displayed on the WFM. Since HD color bars are transmitted, the primary outputs/inputs of each channel should be used.
3. For all channels, configure the clock headers to the programmable clock option.
4. Open the GUI.
5. Select appropriate buttons on the GUI according to *Figure 6-6*. Please note that there are two methods for setting the data rate on the reclocker channels. One method is to select “Auto Rate Detect”, which will reconfigure the programmable clocks to the incoming data rate. The other method is to set the data rate for all reclocked channels to be the same as the data rate of the transmitting channel. In the set up shown in *Figure 6-5* and *Figure 6-6*, the transmitting data rate is 1485 Mb/s which is transmitting HD color bars. All reclocked channels are configured to automatically detect this data rate.
6. Press the “Run” button for channel C, then channel A, then channel B, then channel D.
7. View the picture display of the signal on the WFM 700.

[+] Feedback

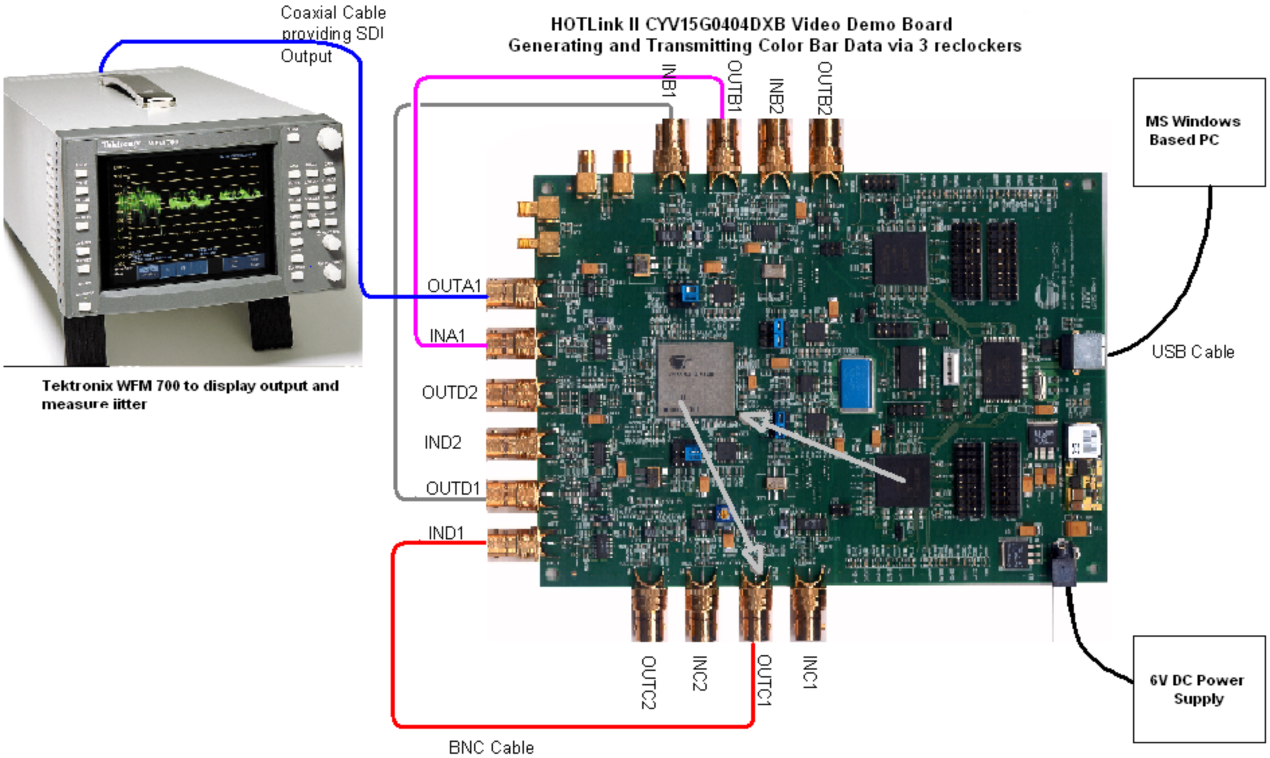


Figure 6-5. Sample Test 2–Transmits Color Bar Data Via Three Reclockers

[+] Feedback

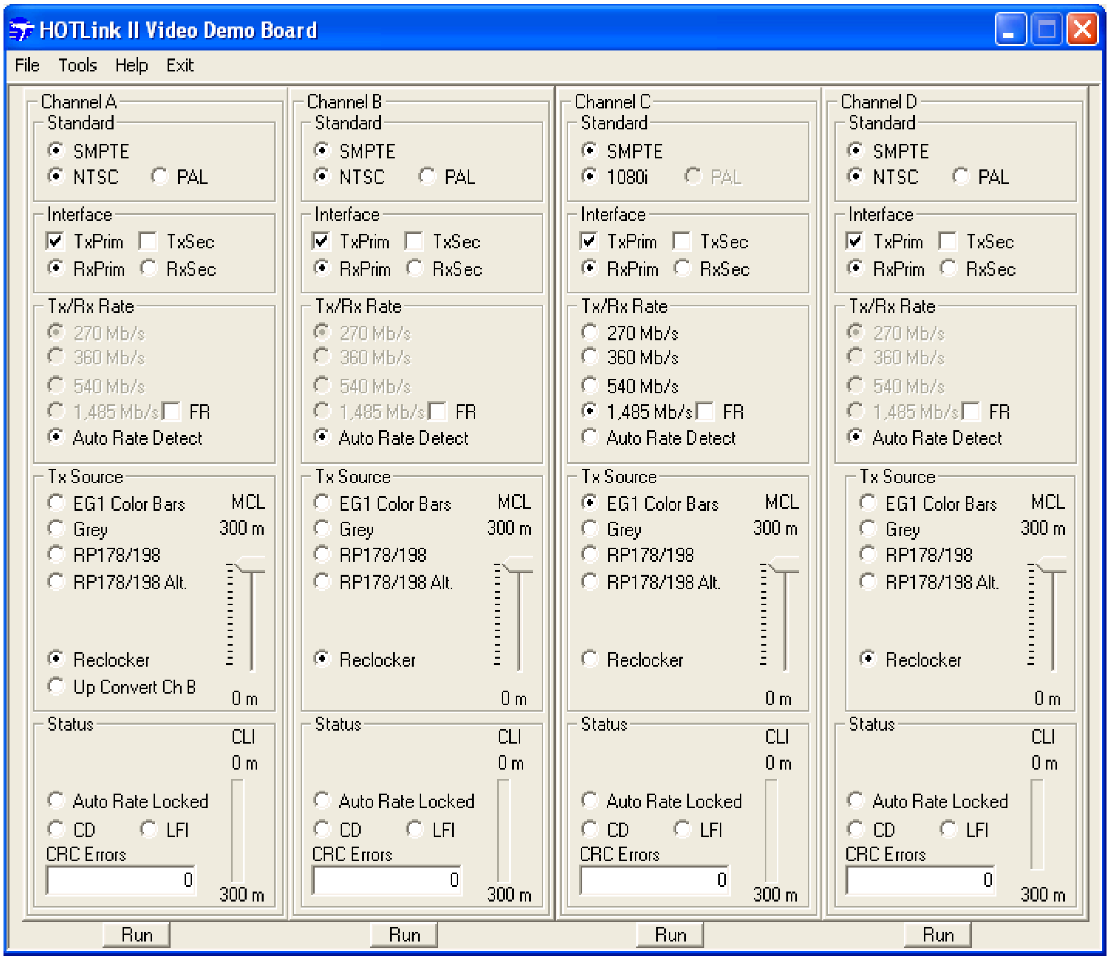


Figure 6-6. GUI Setting for Sample Test 2

6.3.3 *Using Redundant Outputs*

This test shows that primary input/output of a channel on the board supports both SD-SDI and HD-SDI standards while the secondary input/output supports only the SD-SDI standard (due to presence of SD-SDI equalizers and cable drivers on secondary I/Os).

1. Apply power to the board and connect the USB cable between the board and the computer.
2. Connect output OUTB1 to the WFM 700 channel A input and connect output OUTB2 to the WFM 700 channel B input using BNC cables.
3. Open the GUI.
4. Select the appropriate GUI settings according to *Figure 6-8*. For this setting, channel B is transmitting SD-SDI color bars on both primary and secondary outputs.
5. Press the “Run” button for channel B.
6. Press the “Input” button on the WFM to display either the primary or secondary output.
7. Press the “Stop” button for channel B.
8. Change the GUI settings according to *Figure 6-9*. For this setting, channel B is transmitting HD-SDI color bars only on the primary output.
9. Press the “Run” button for channel B.
10. Press the Input button on the WFM 700 to display either the primary or secondary output. No signal is shown when the secondary output is selected.

[+] Feedback

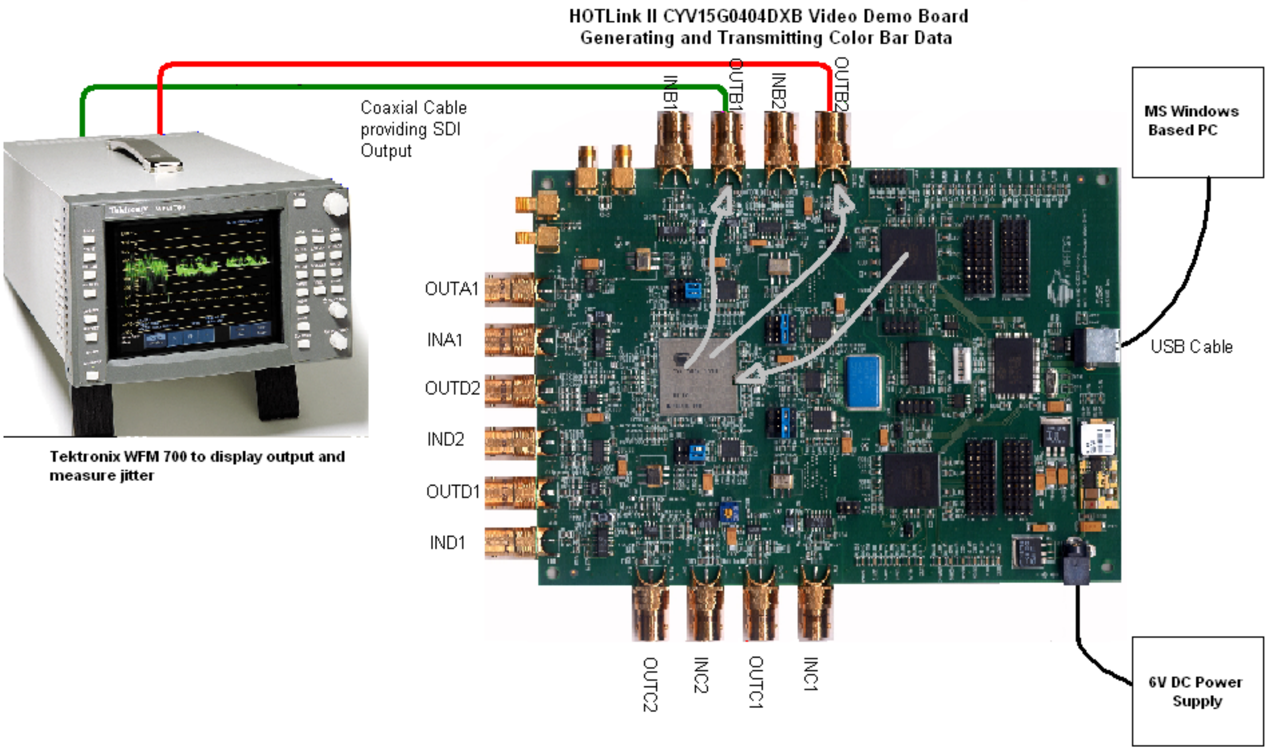


Figure 6-7. Sample Test 3–Generate and Transmit Color Bars Through Both Output Buffers

[+] Feedback

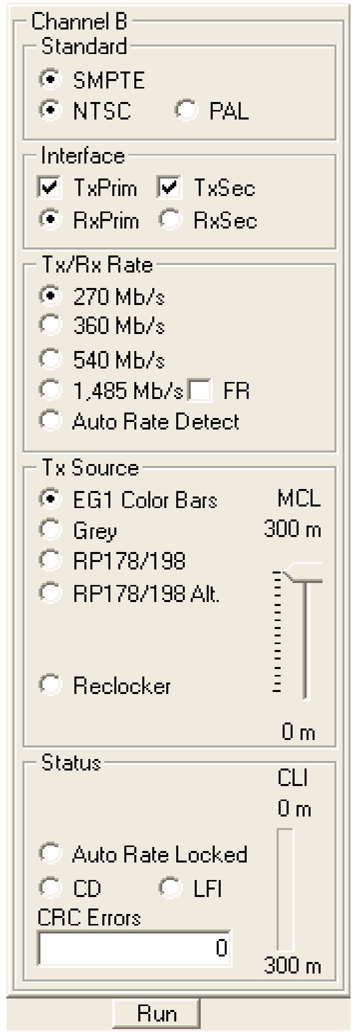


Figure 6-8. GUI Setting for Sample Test 3–Transmit SD-SDI Color Bars

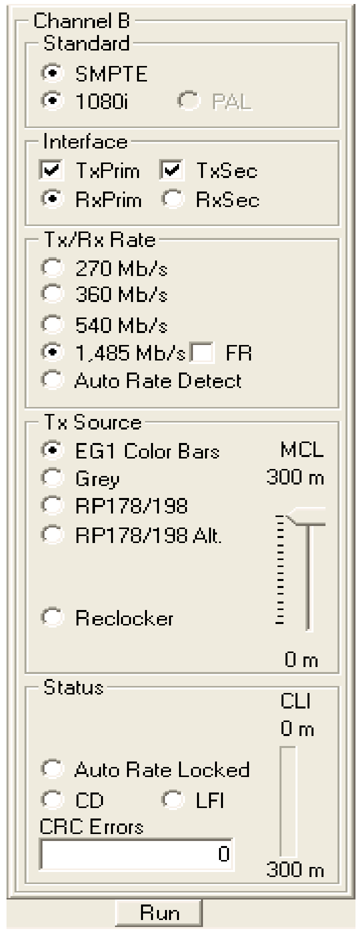


Figure 6-9. GUI Setting for Sample Test 3–Transmit HD-SDI Color Bars

6.3.4 Using Selectable Inputs and Automatic Rate Detection

1. Apply power to the board and connect the USB cable between the board and the computer.
2. Connect OUTB1 to IND2, OUTA1 to IND1, and OUTD1 to input A of the WFM 700.
3. Configure the clock header for channel A to the 74.25-MHz on-board crystal oscillator option, the clock header for channel B and channel D to the programmable clock option.
4. Open the GUI
5. Configure channel A to generate the grey pattern in HD format at 1485 Mb/s and channel B to generate the EG1 color bars in SD format at 270 Mb/s. For channel D, select TxPrim and RxPrim with Auto Rate Detect and Reclocker enabled. See *Figure 6-11*.
6. Press the “Run” button for channel A, channel B, and channel D.
7. View the picture display of the signal on the WFM 700. The user should see the grey pattern in HD-SDI format displayed.
8. Press the “Stop” button for channel D.
9. Keep the GUI settings for channel A and channel B. For channel D, select TxPrim and RxSec with Auto Rate Detect and Reclocker enabled. See *Figure 6-12*.
10. Press the “Run” button for channel A, channel B, and channel D.
11. View the picture display of the signal on the WFM 700. The user should see the EG1 color bars in SD-SDI format displayed.
12. Press the “Stop” button for all channels.
13. Keep the GUI settings for channel A and channel B. For channel D, keep the settings in the “Interface” panel; select the data rate to be 270 Mb/s and reclocker enabled. See *Figure 6-13*.
14. Press the “Run” button for channel A, channel B, and channel D.

[+] Feedback

15.View the picture display of the signal on the WFM 700. The user should see the EG1 color bars in SD-SDI format displayed.

16.Press the "Stop" button for all channels.

Note: For this test, the clock headers for channel A can be configured to either the on-board programmable clock option or the on-board 74.25-MHz crystal oscillator clock option. Clock headers for channel B and channel D should be configured to the on-board programmable clock option.

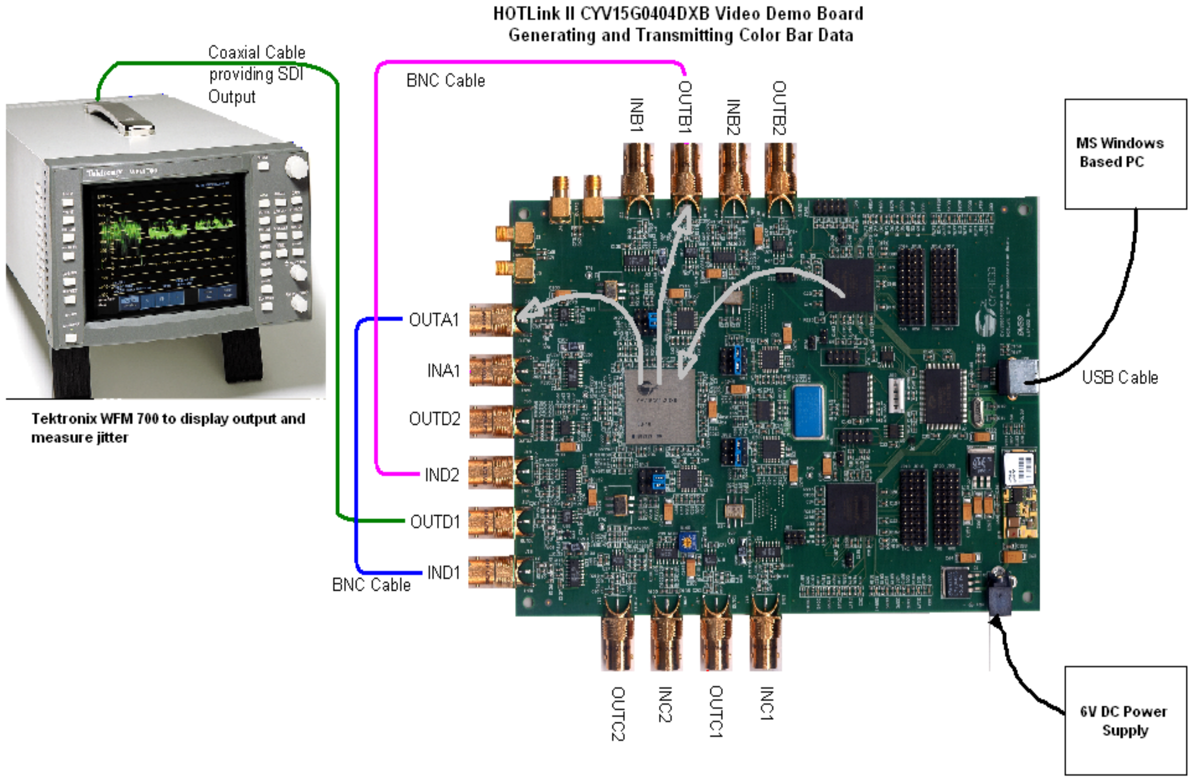


Figure 6-10. Sample Test 4–Selectable Inputs and Auto Rate Detection

[+] Feedback

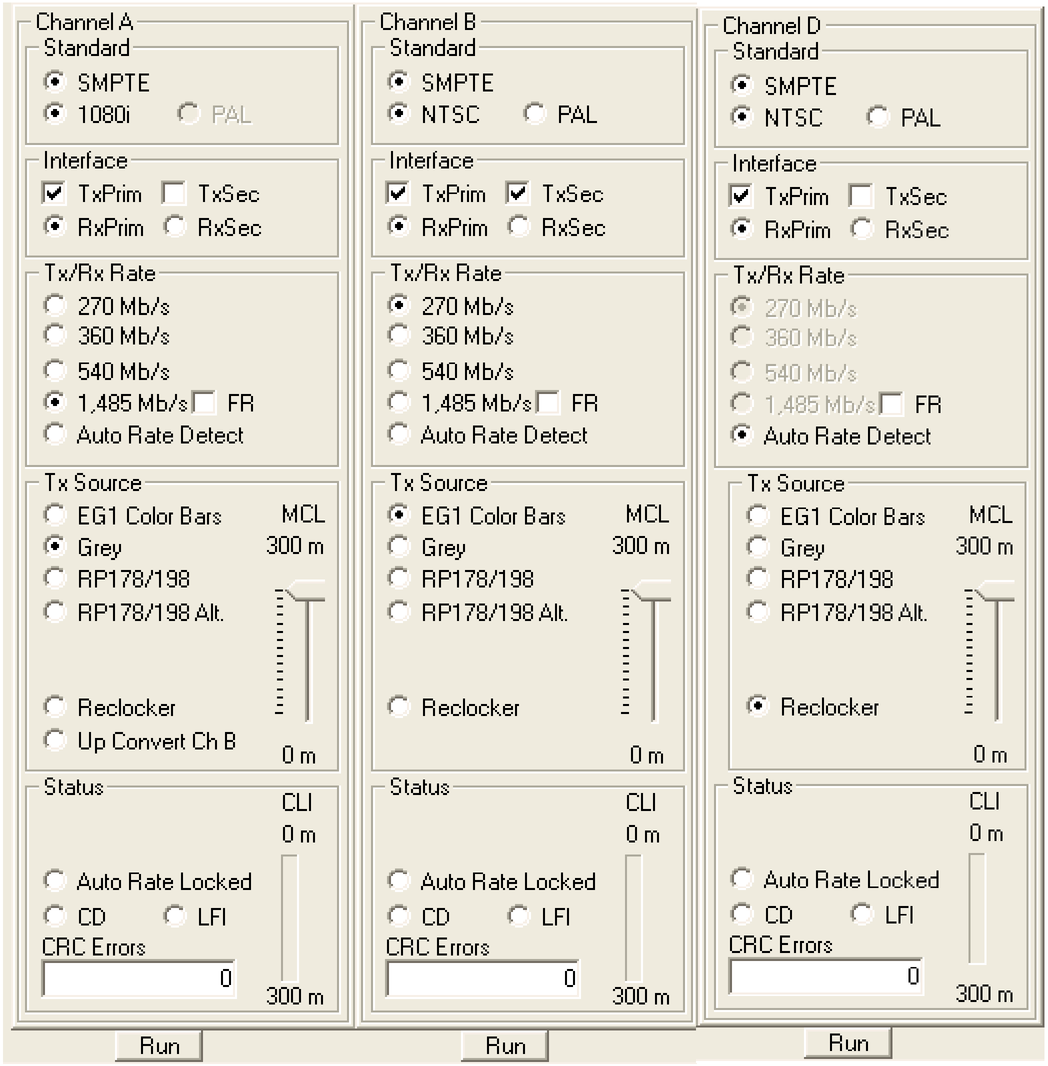


Figure 6-11. GUI Setting for Sample Test 4: Step 6

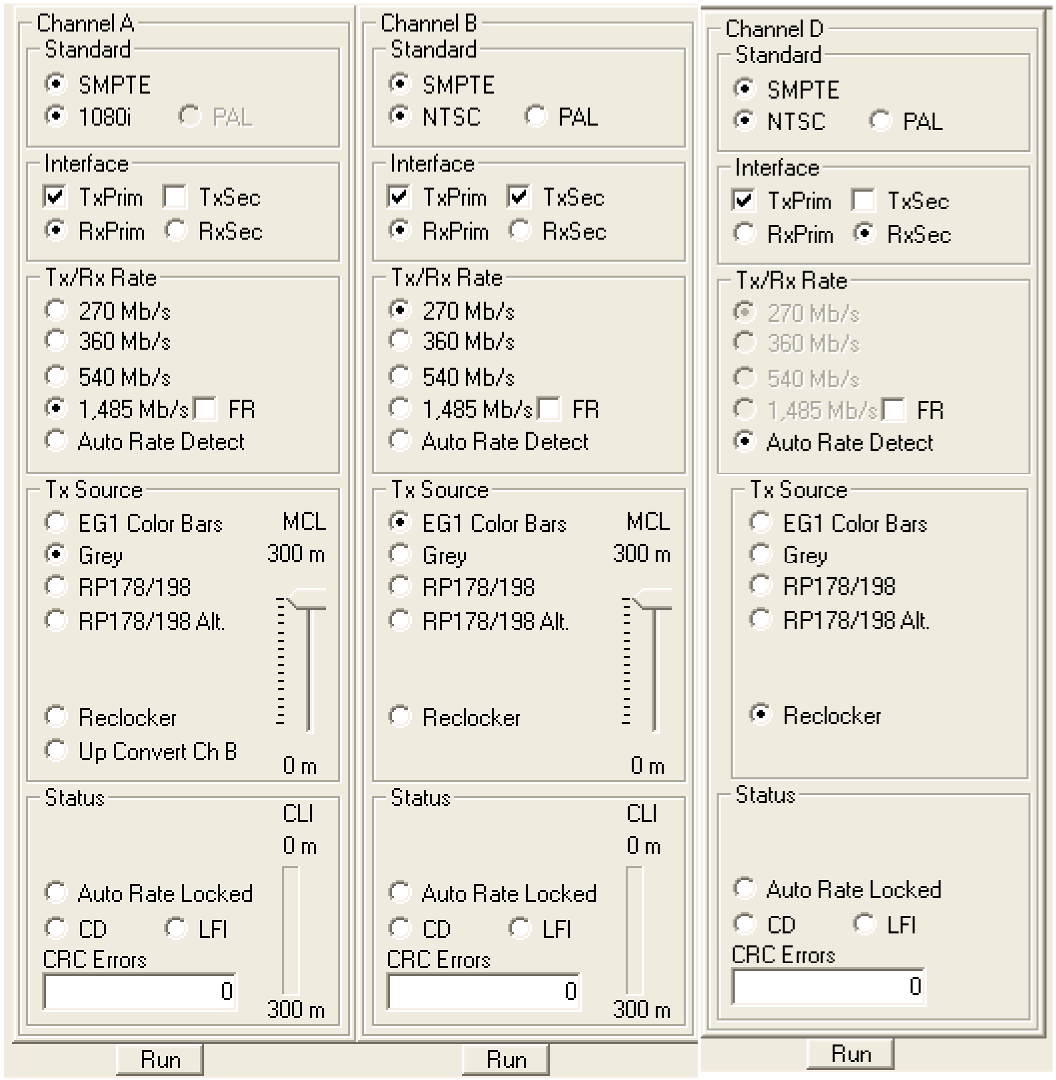


Figure 6-12. GUI Settings for Sample Test 4: Step 9

[+] Feedback

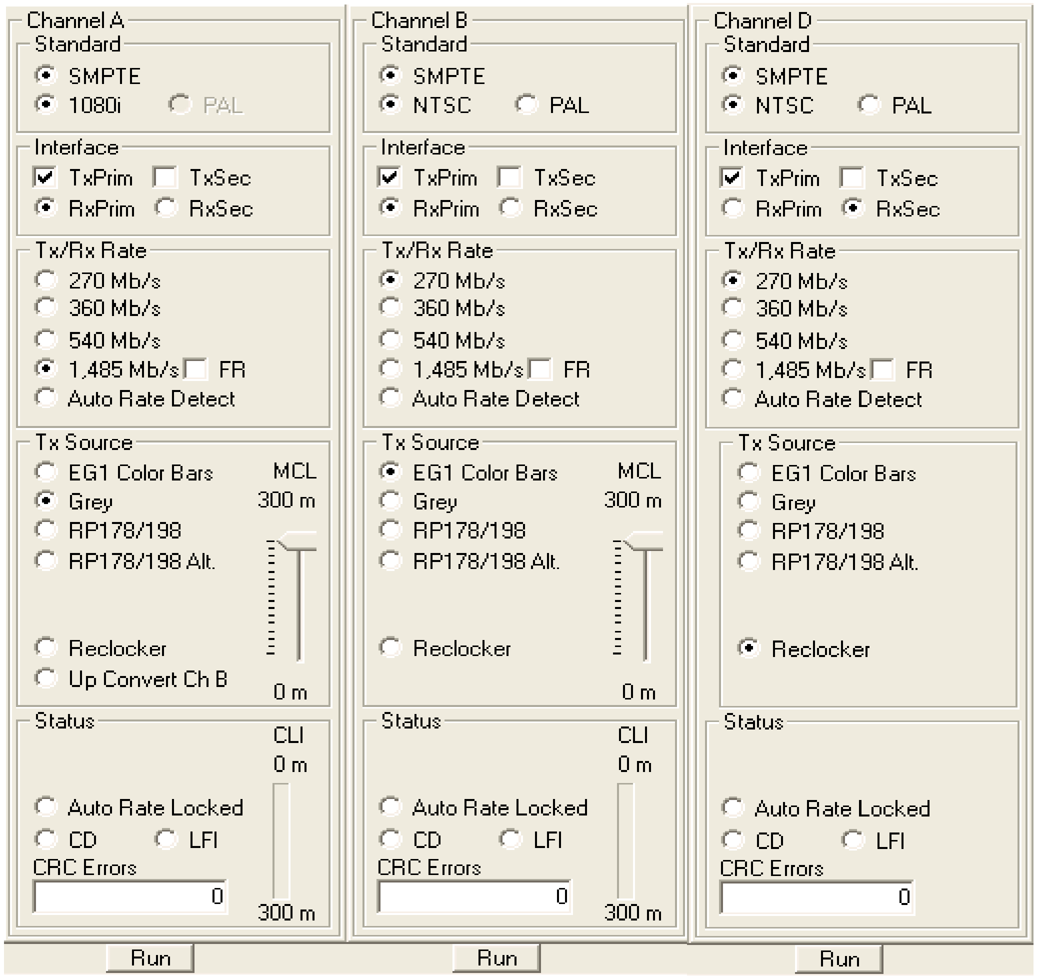


Figure 6-13. GUI Setting for Sample Test 4: Step 13

7.0 Summary

The Cypress HOTLink II family of transceivers are compliant to requirements specified by SMPTE for SD-SDI and HD-SDI serial interfaces. The evaluation platform provides a full-fledged reference design that enables customers to easily implement Serial Digital Interface systems with HOTLink II Video PHYs.

8.0 References

1. *Television—10-Bit 4:2:2 Component and 4fsc Composite Digital Signals–Serial Digital Interface*, ANSI/SMPTE 259M–1997, Society of Motion Picture and Television Engineers, 1997.
2. *Television—Component Video Signal 4:2:2 - Bit-Parallel Digital Interface*, ANSI/SMPTE 125M-1995, Society of Motion Picture and Television Engineers, 1995.
3. *Television—System M/NTSC Composite Video Signals–Bit-Parallel Digital Interface*, ANSI/SMPTE 244M-1995, Society of Motion Picture and Television Engineers, 1995.
4. *Television—Bit-Parallel Digital Interface–Component Video Signal 4:2:2 16x9 Aspect Ratio*, ANSI/SMPTE 267M-1995, Society of Motion Picture and Television Engineers, 1995.
5. *Pathological Conditions in Serial Digital Video Systems*, SMPTE Engineering Guidelines, EG 34-1999, Society of Motion Picture and Television Engineers, 1999.
6. *Serial Digital Interface Checkfield for 10-Bit 4:2:2 Component and 4fsc Composite Digital Signals*, SMPTE Recommended Practices, RP 178-1996, Society of Motion Picture and Television Engineers, 1996.
7. SDI SMPTE Jitter Performance of the Independent Channel HOTLink II™ Transceiver, Application Note, Cypress Semiconductor Corporation 2004.

[+] Feedback

Appendix A: Schematics of HOTLink II CYV15G0404DXB Video Demo Board

[+] Feedback

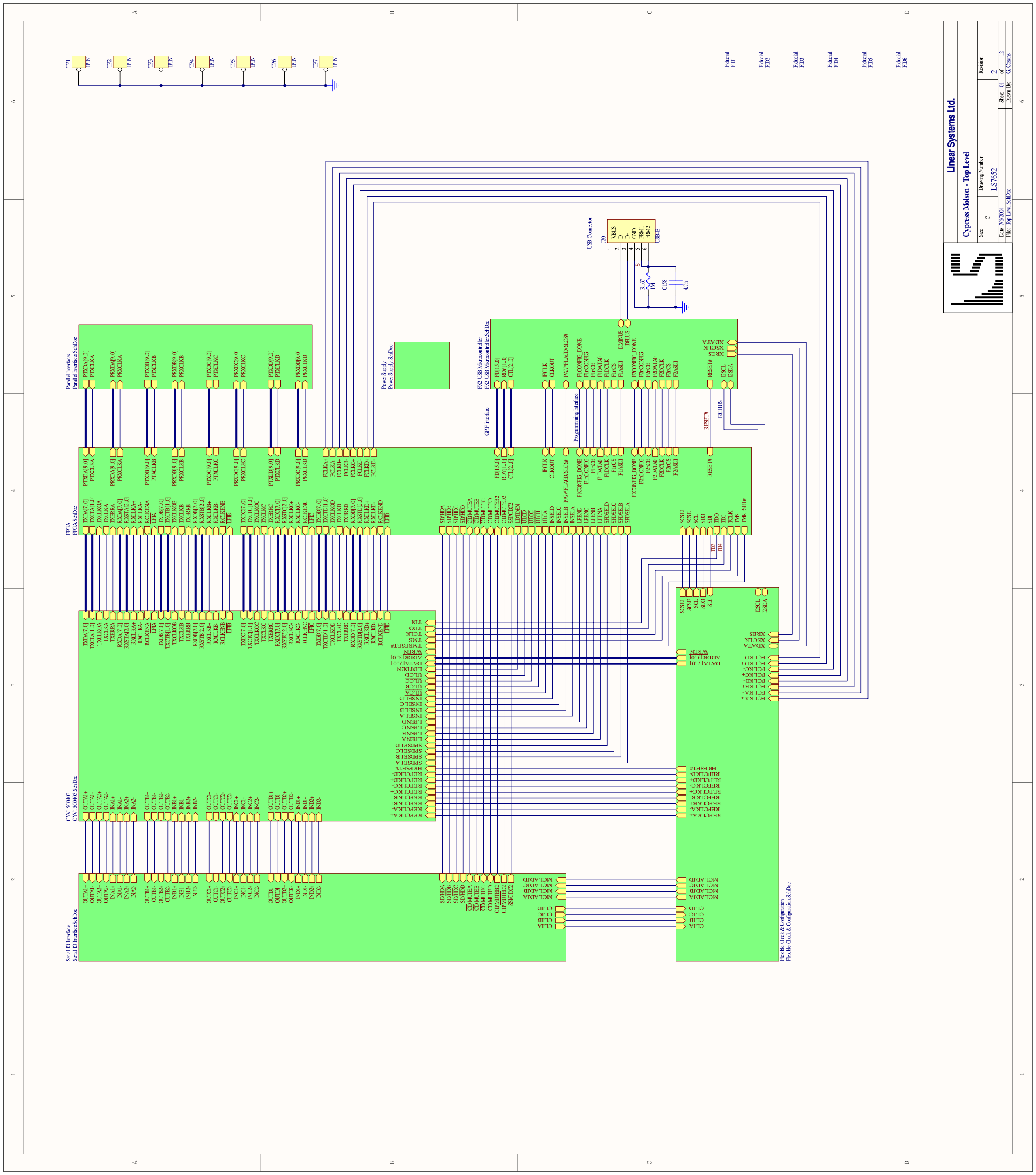


Figure A-1. Top Level Schematic

[+] Feedback

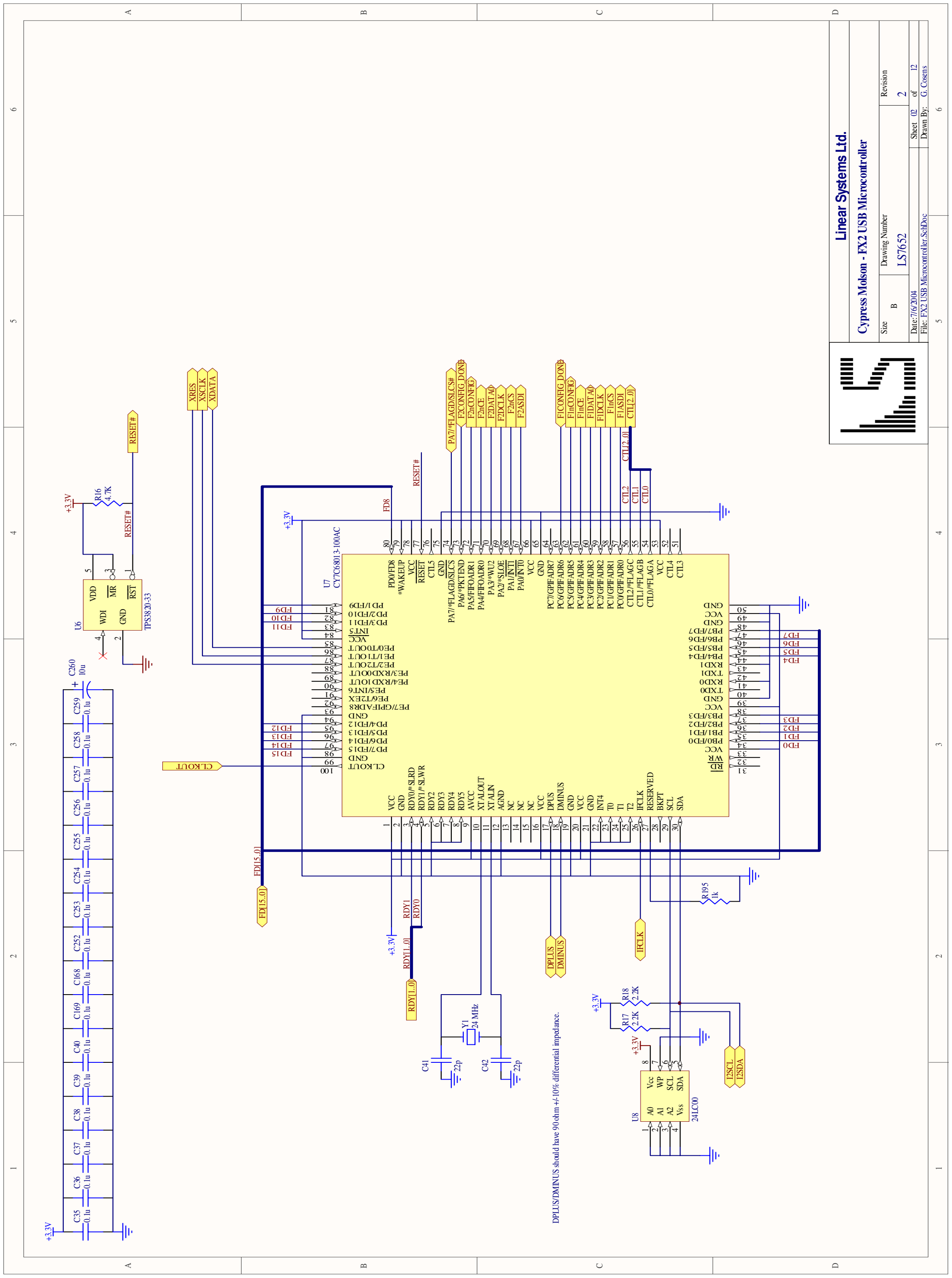


Figure A-2. USB FX2 Microcontroller

[+] Feedback

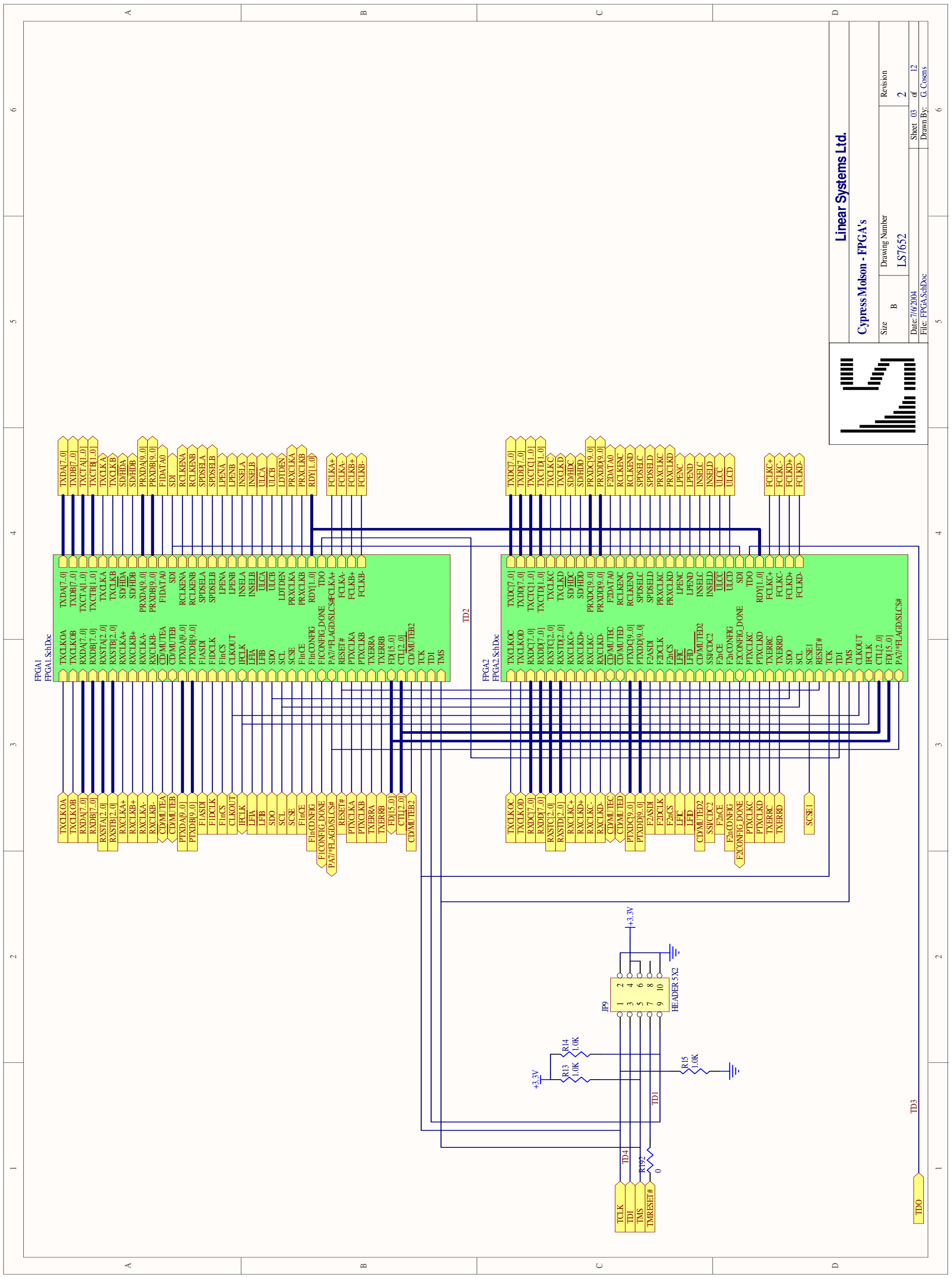


Figure A-3. FPGA Top Level

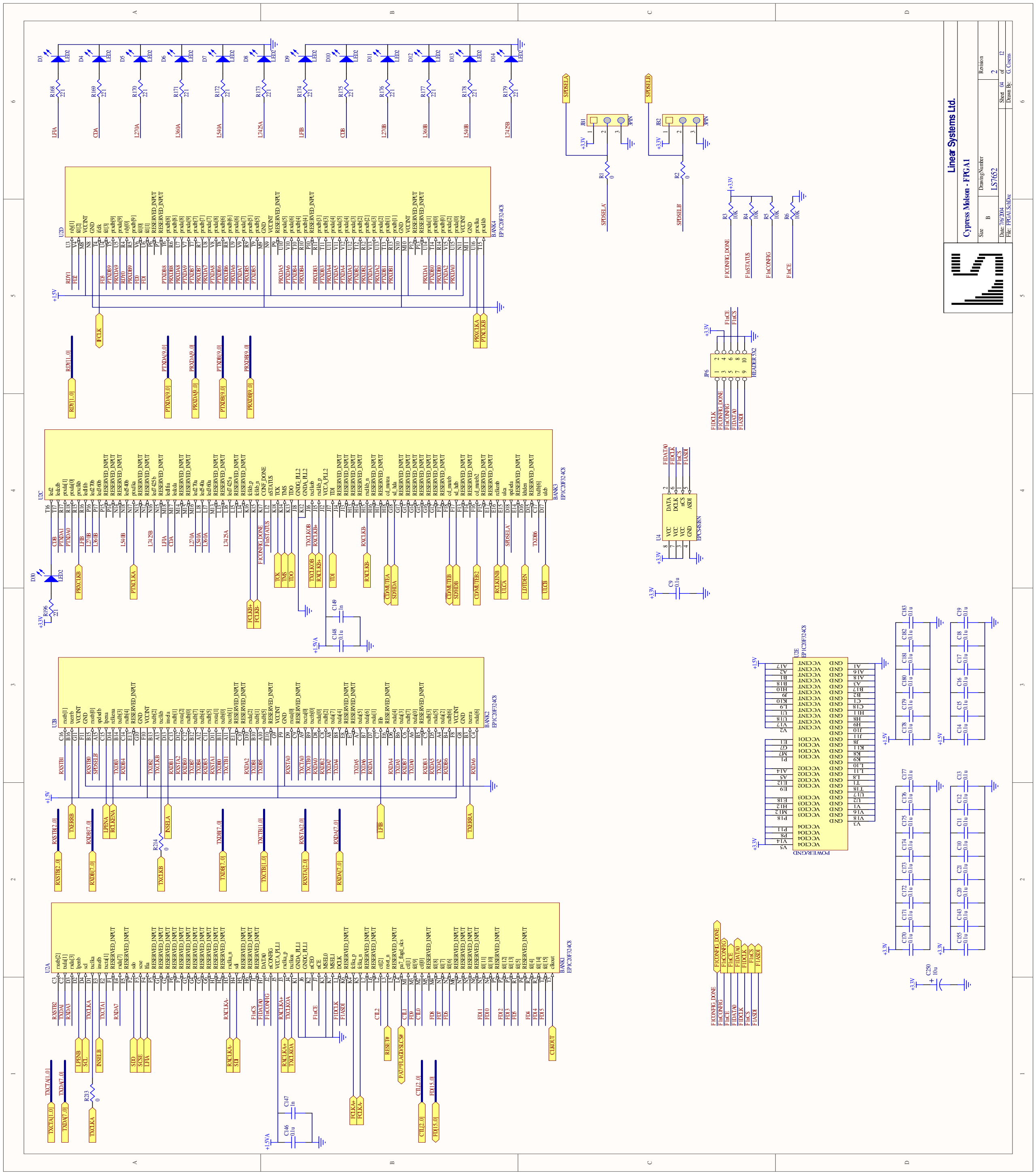


Figure A-4. FPGA for Channel A and B

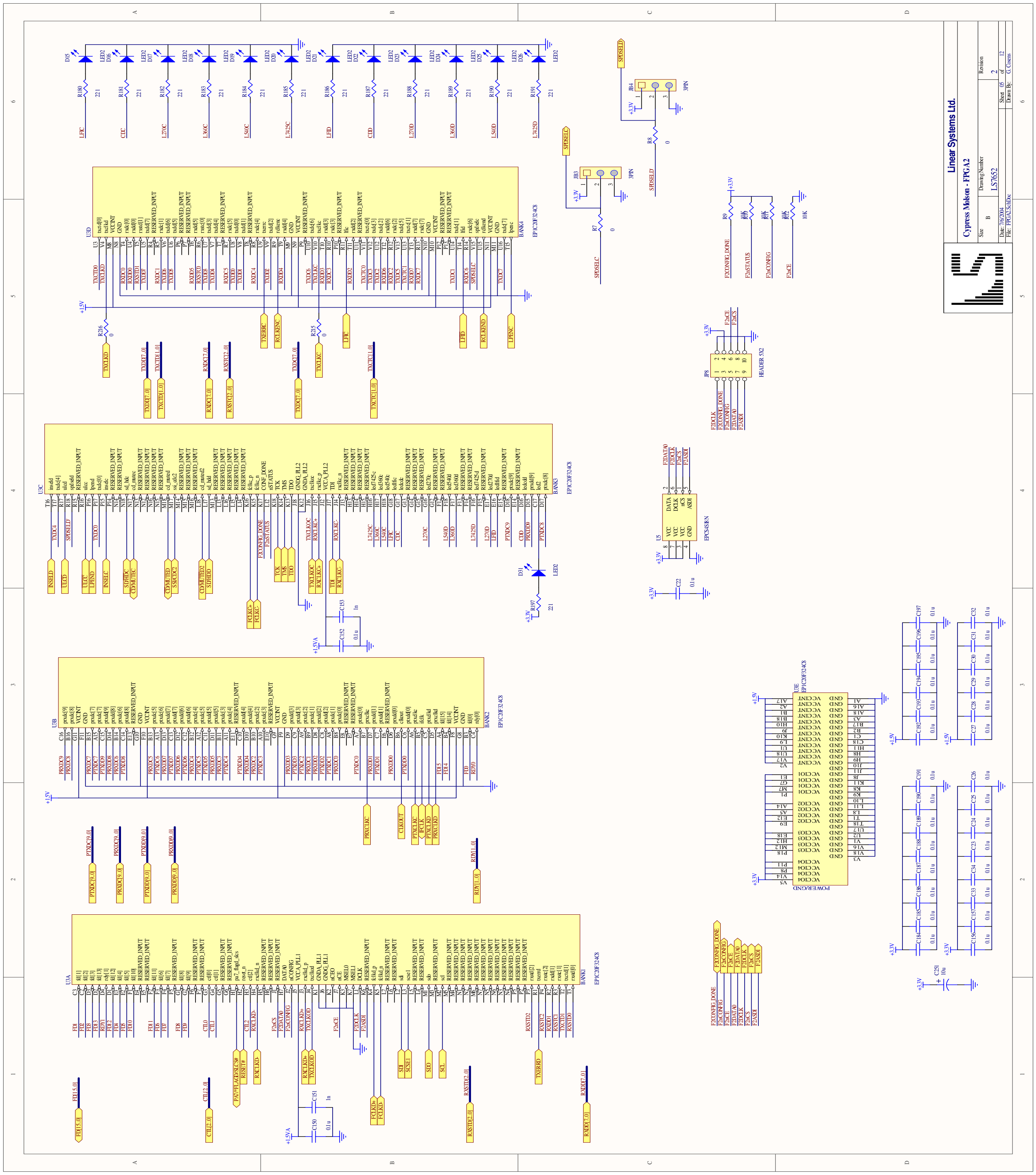


Figure A-5. FPGA for Channel C and D

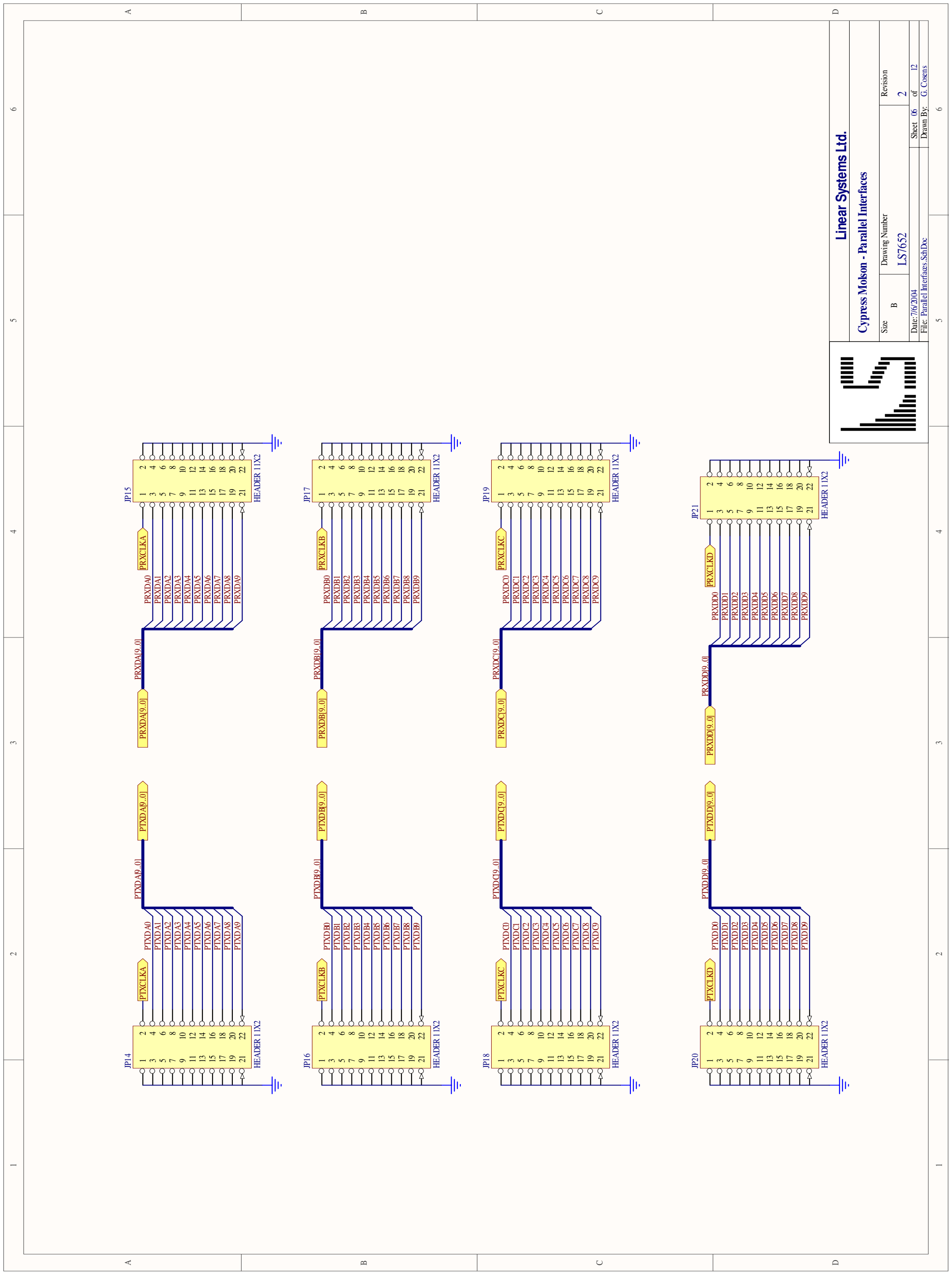


Figure A-6. Parallel Interface Headers

[+] Feedback

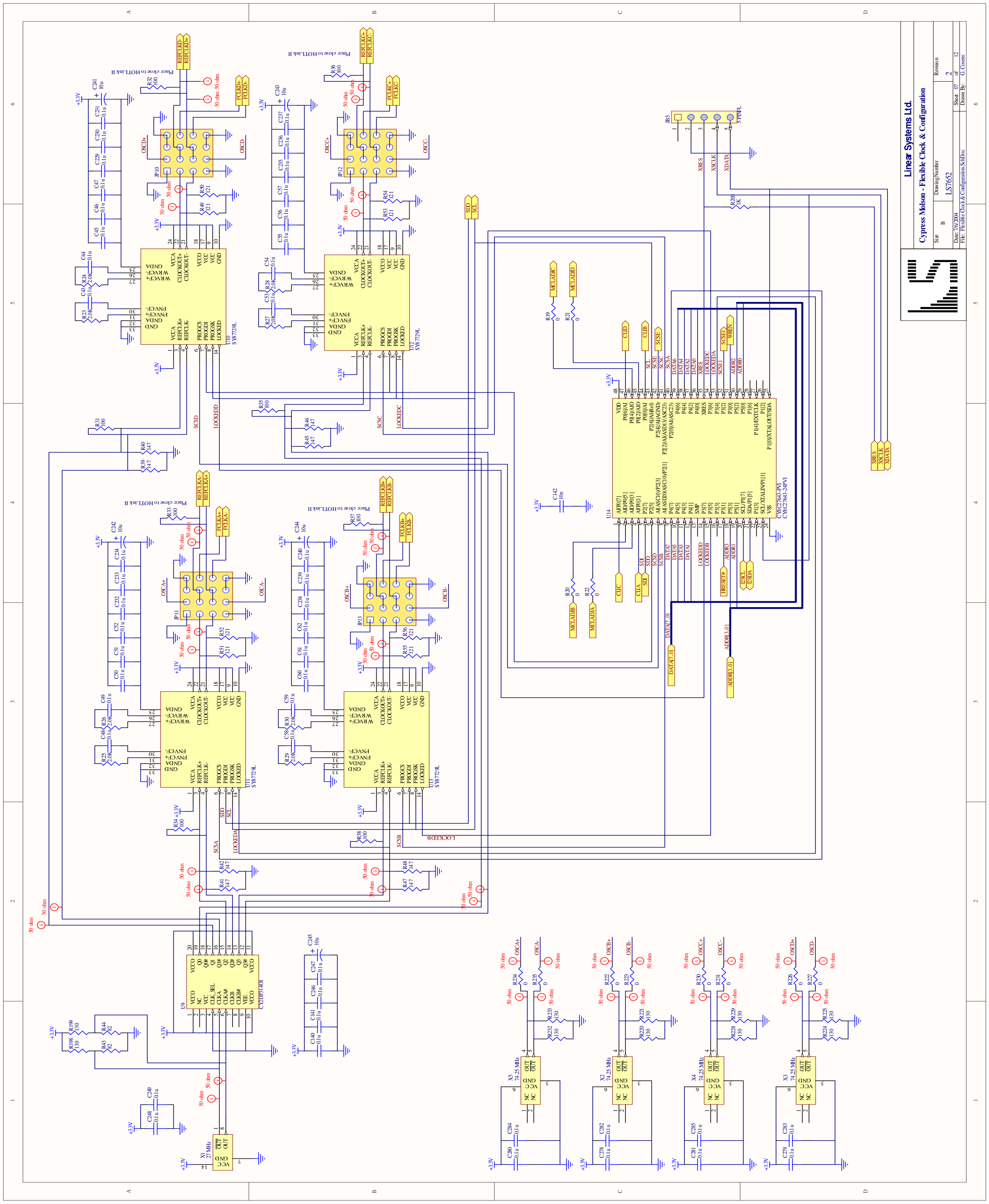


Figure A-7. Clocking and PSoC

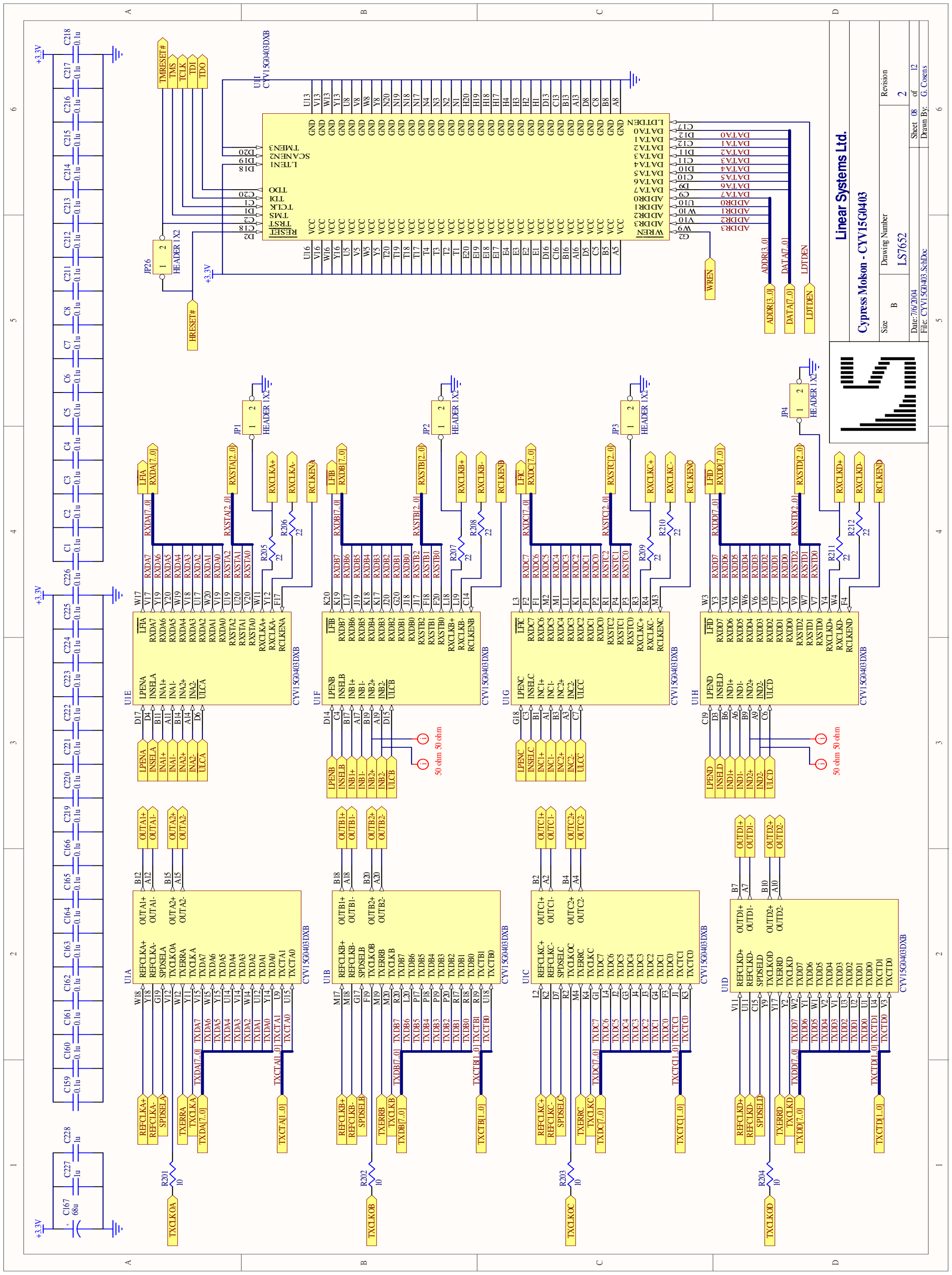


Figure A-8. HOTLink II CYV15G0404DXB

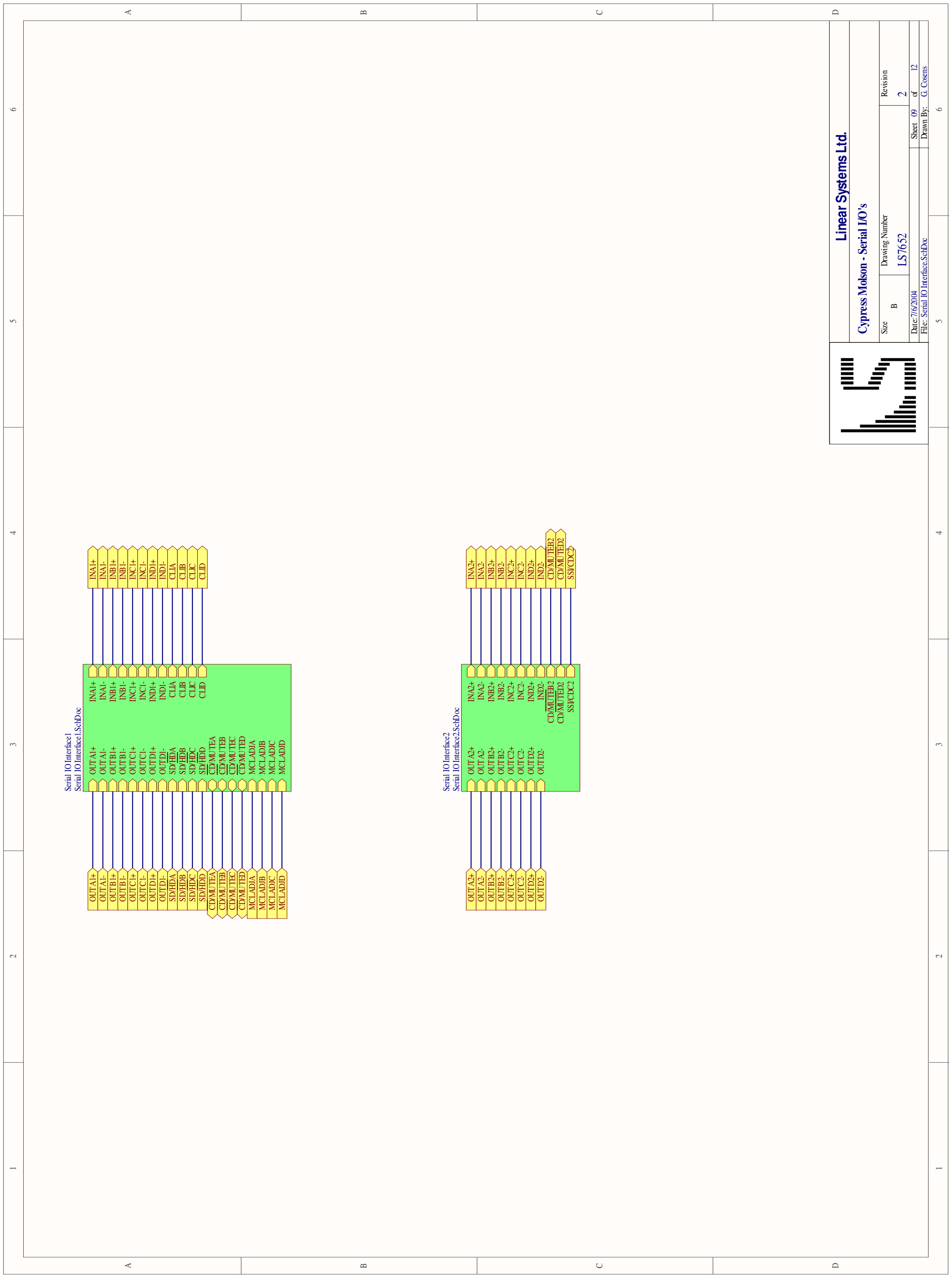


Figure A-9. Serial I/Os Top Level

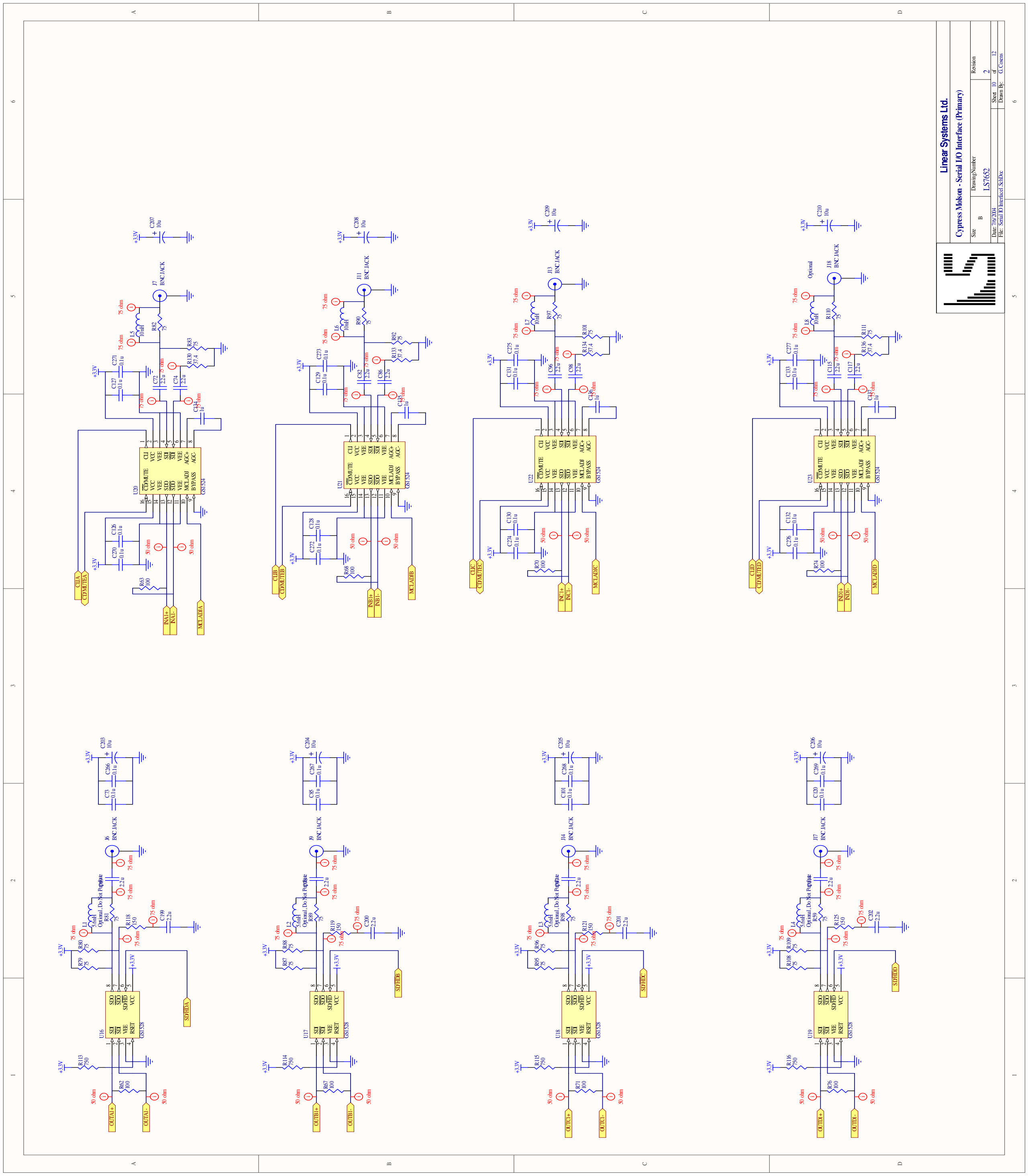


Figure A-10. Serial I/O Interface (Primary)

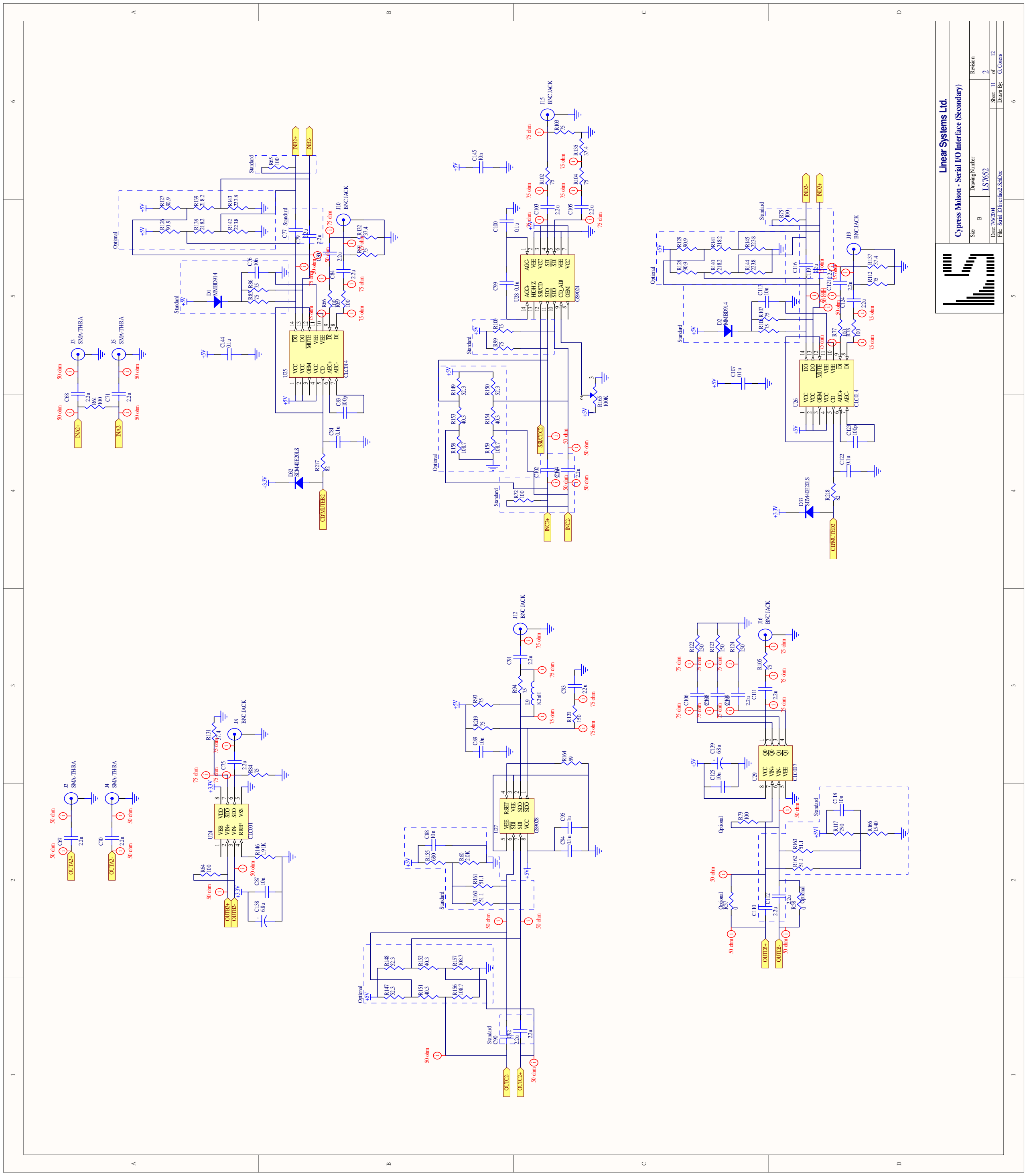


Figure A-11. Serial I/O Interface (Secondary)

[+] Feedback

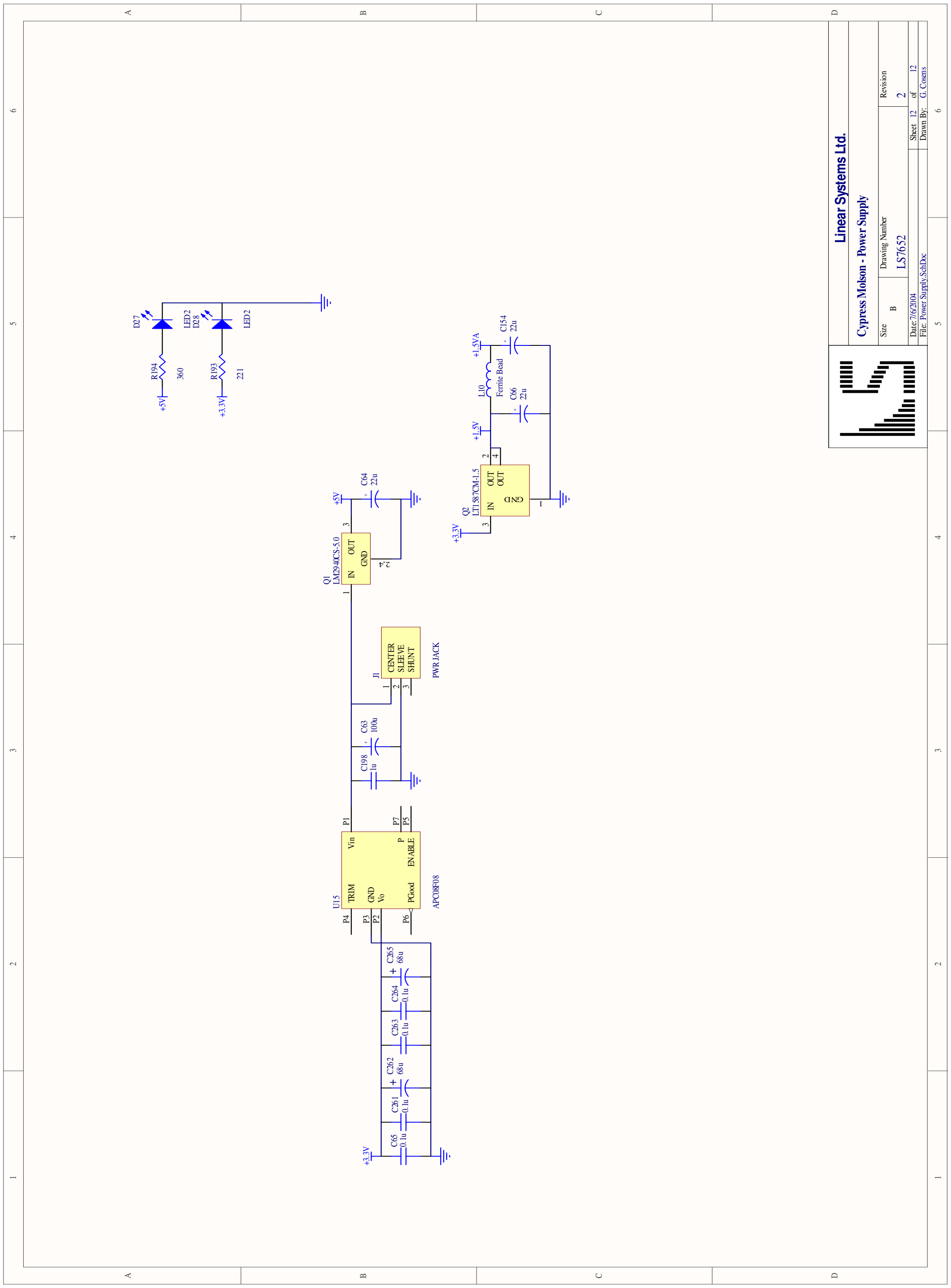


Figure A-12. Power Supply

[+] Feedback

Appendix B: PCB Manufacturing Files (GERBER Files)

[+] Feedback

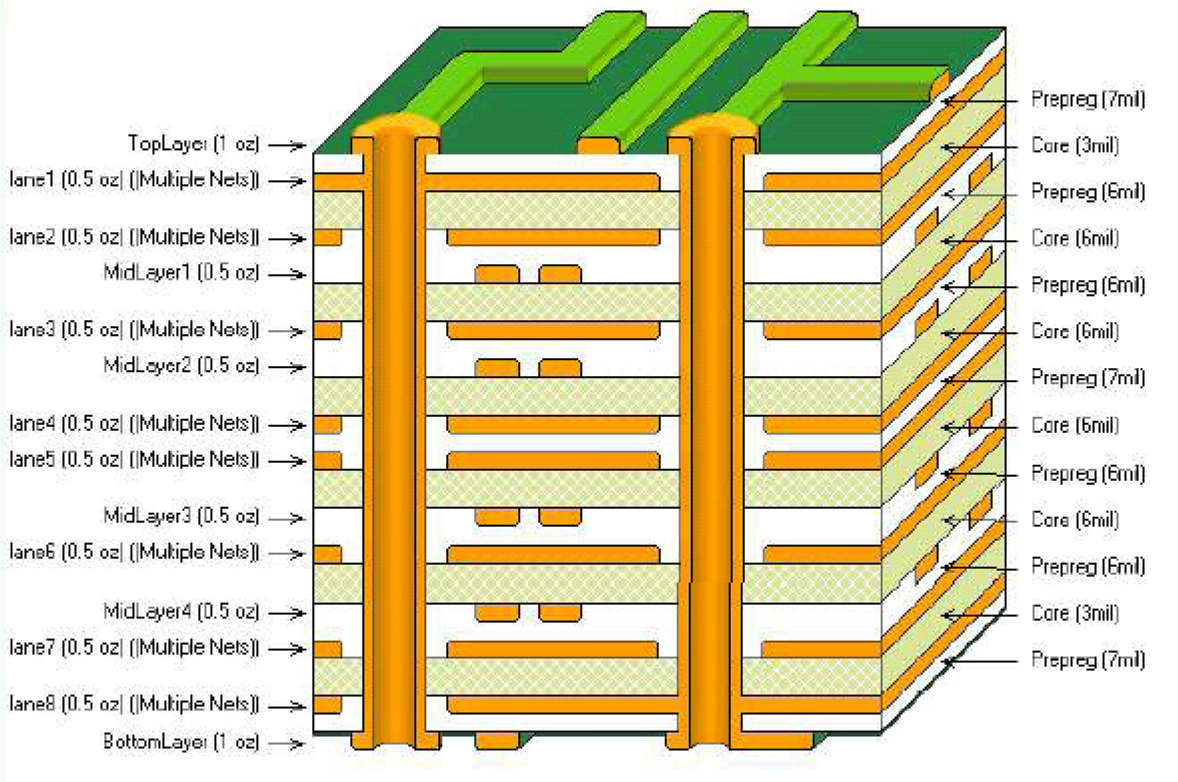


Figure B-1. Board Stackup

[+] Feedback

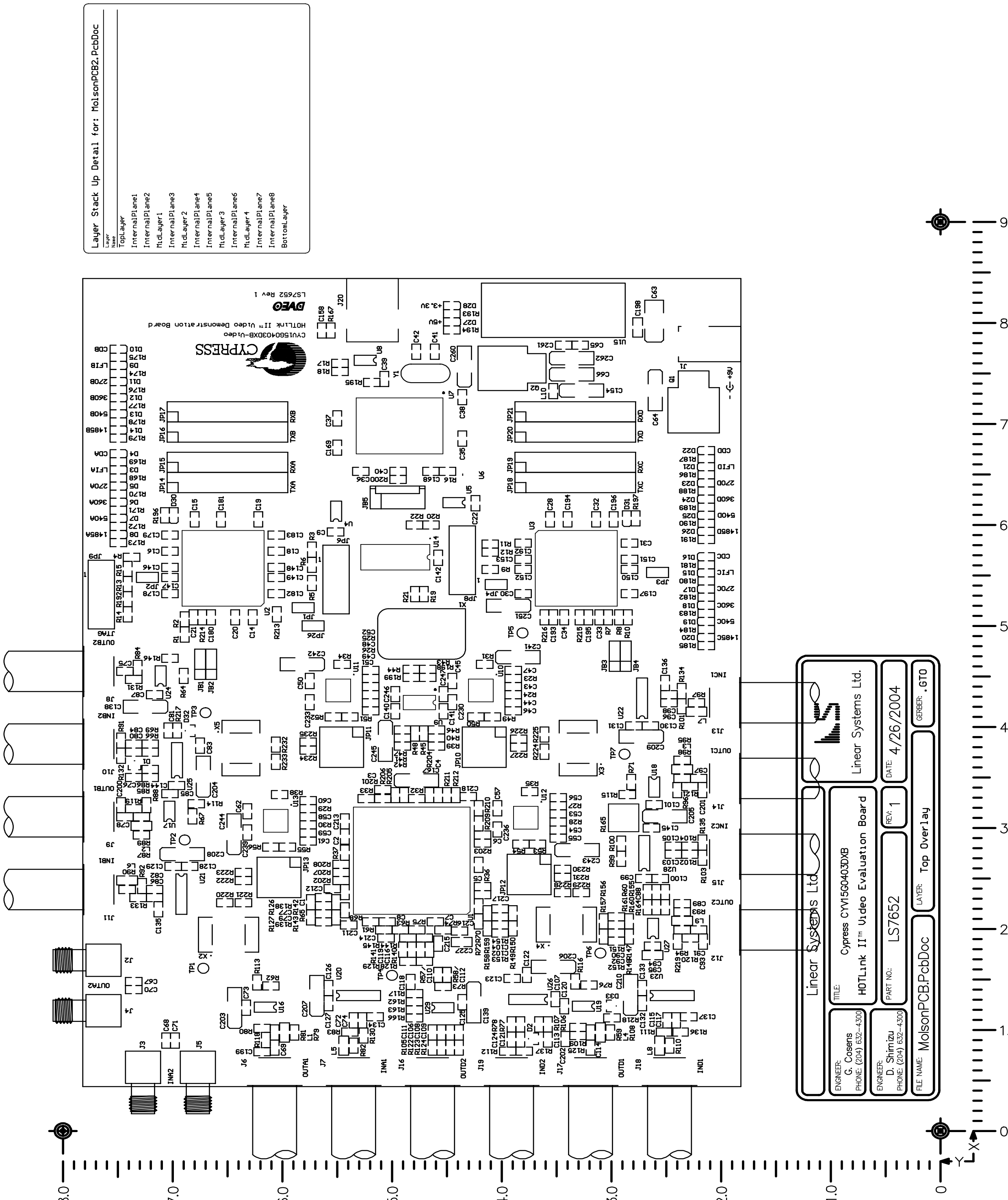


Figure B-2. Top Overlay

[+] Feedback

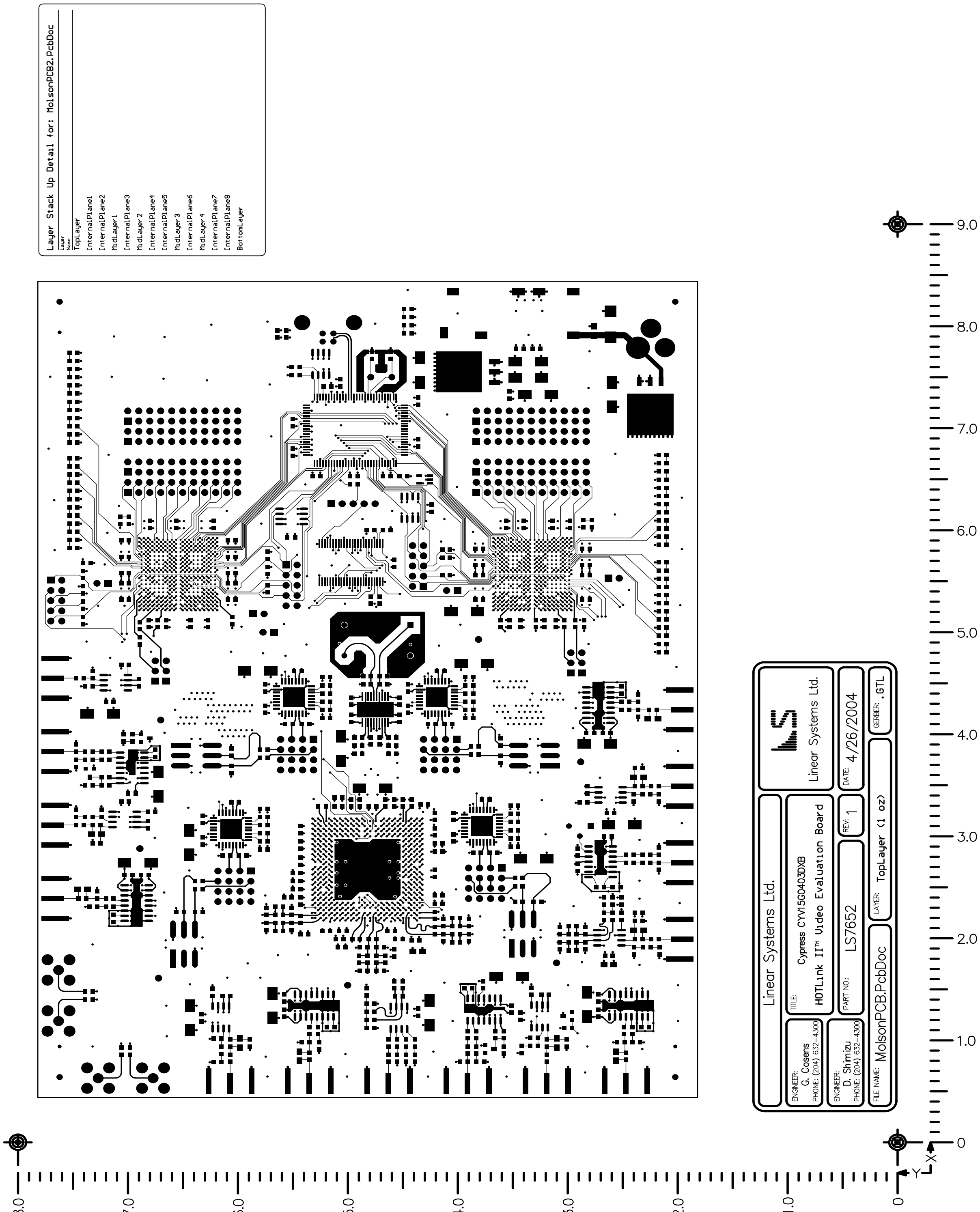


Figure B-3. Top Layer

[+] Feedback

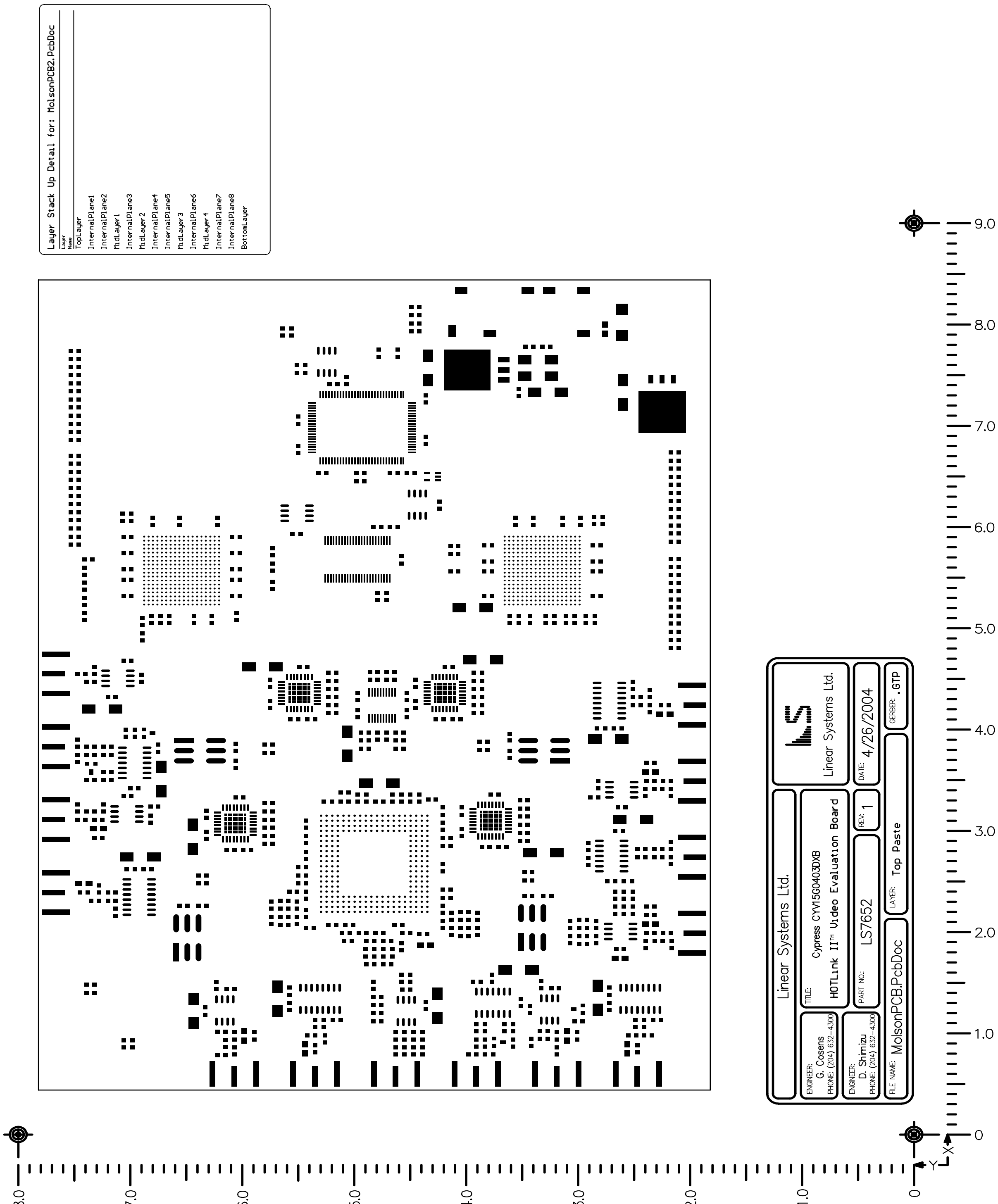


Figure B-4. Top Paste

[+] Feedback

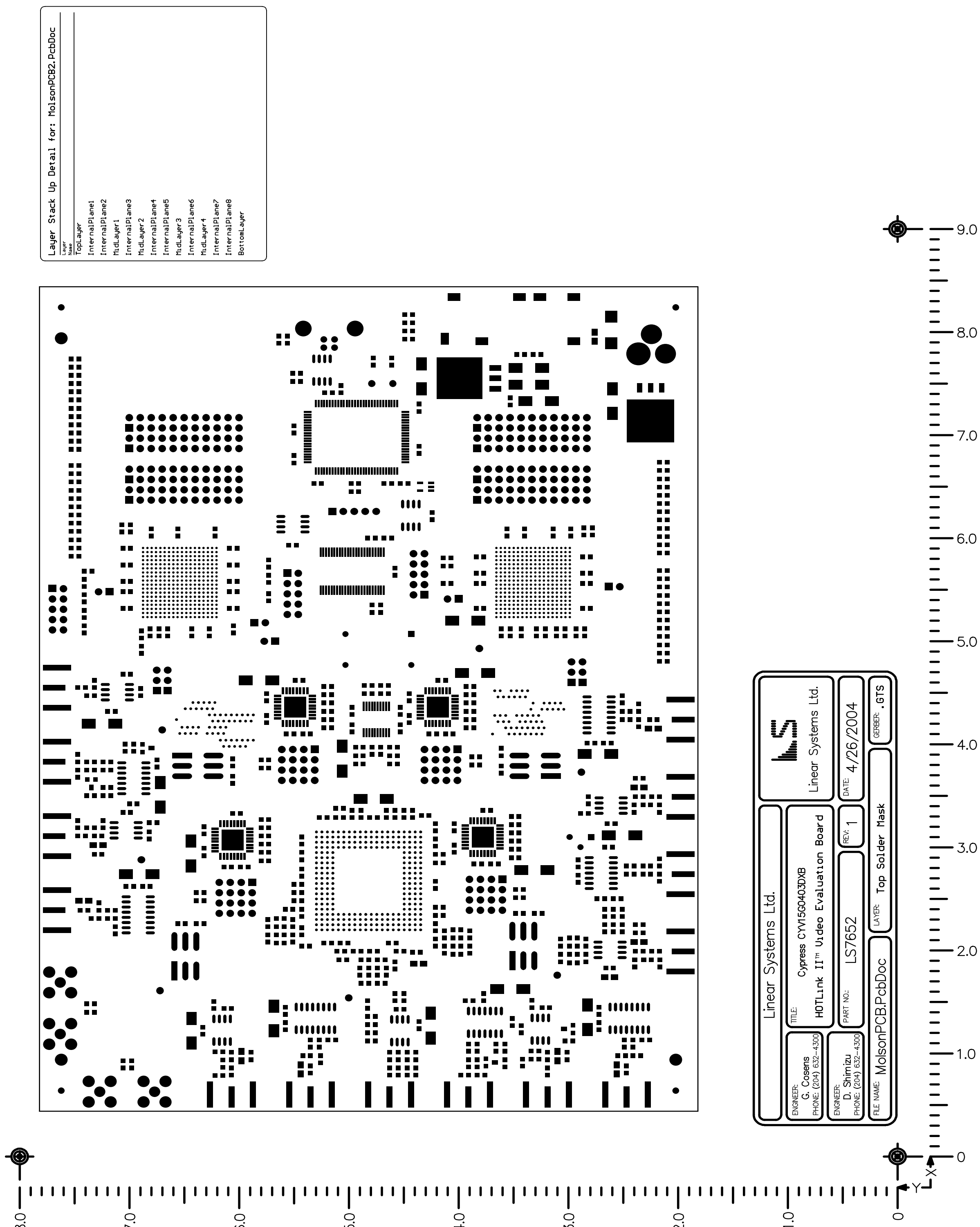


Figure B-5. Top Solder Mask

[+] Feedback

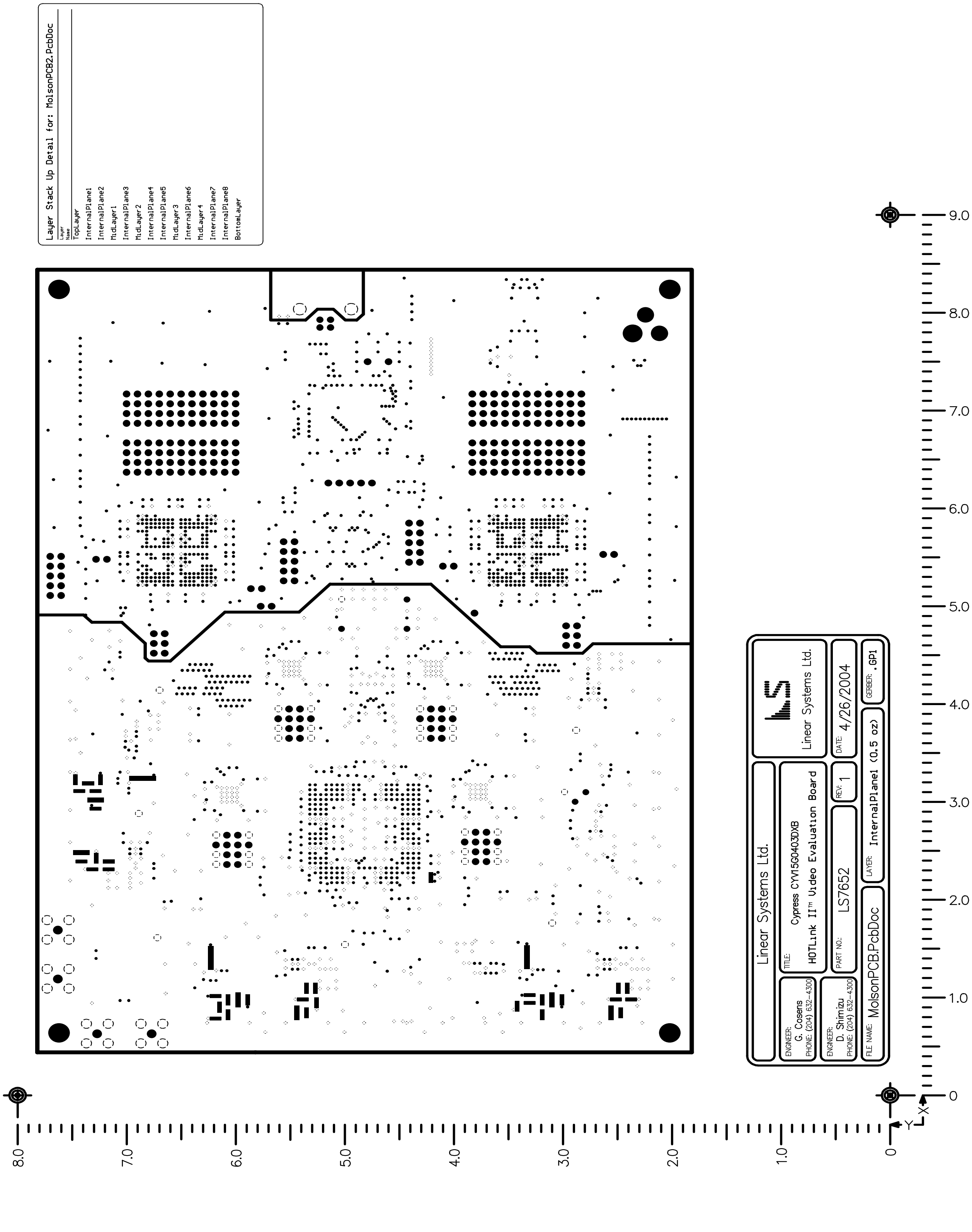


Figure B-6. Internal Plane 1

[+] Feedback

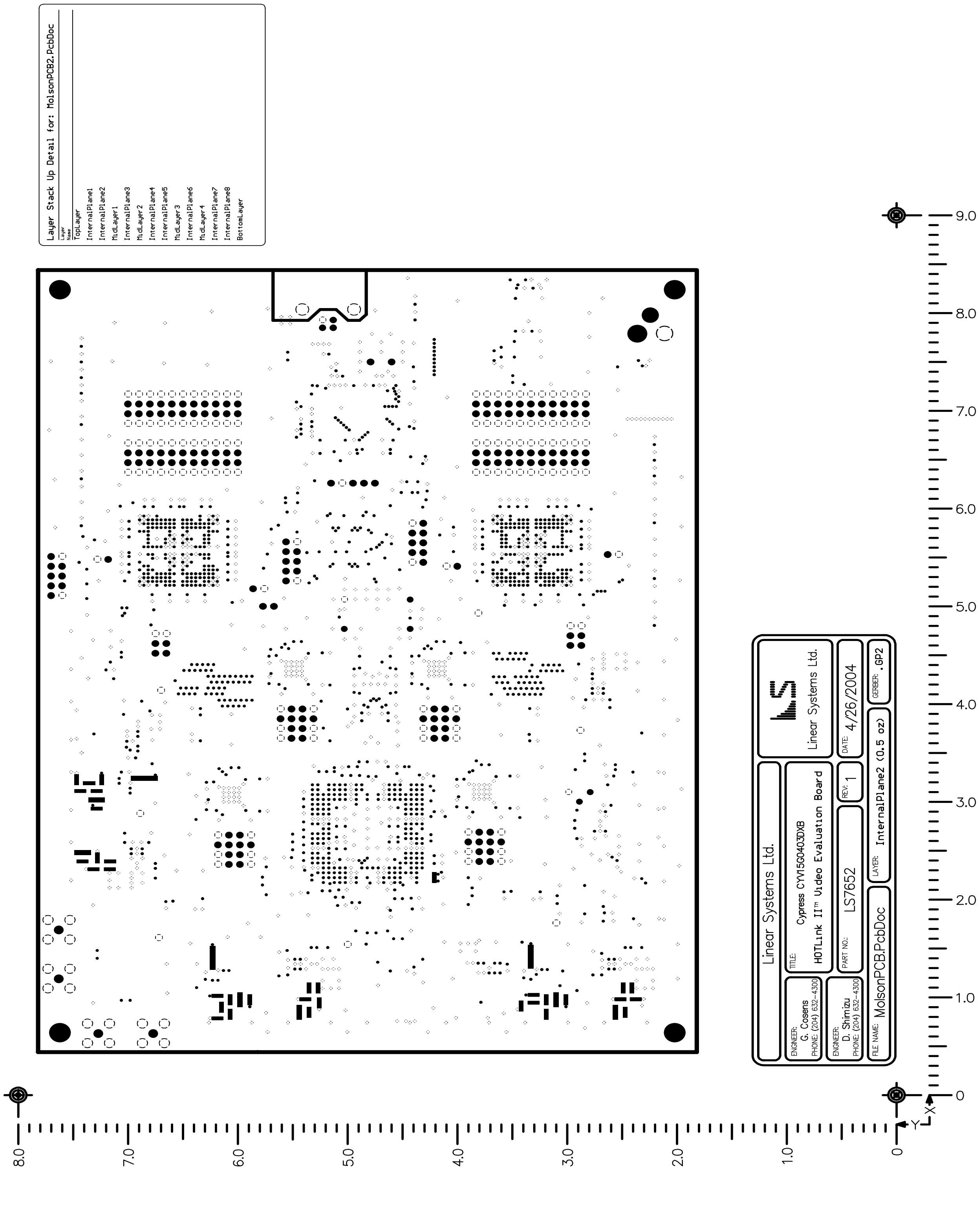


Figure B-7. Internal Plane 2

[+] Feedback

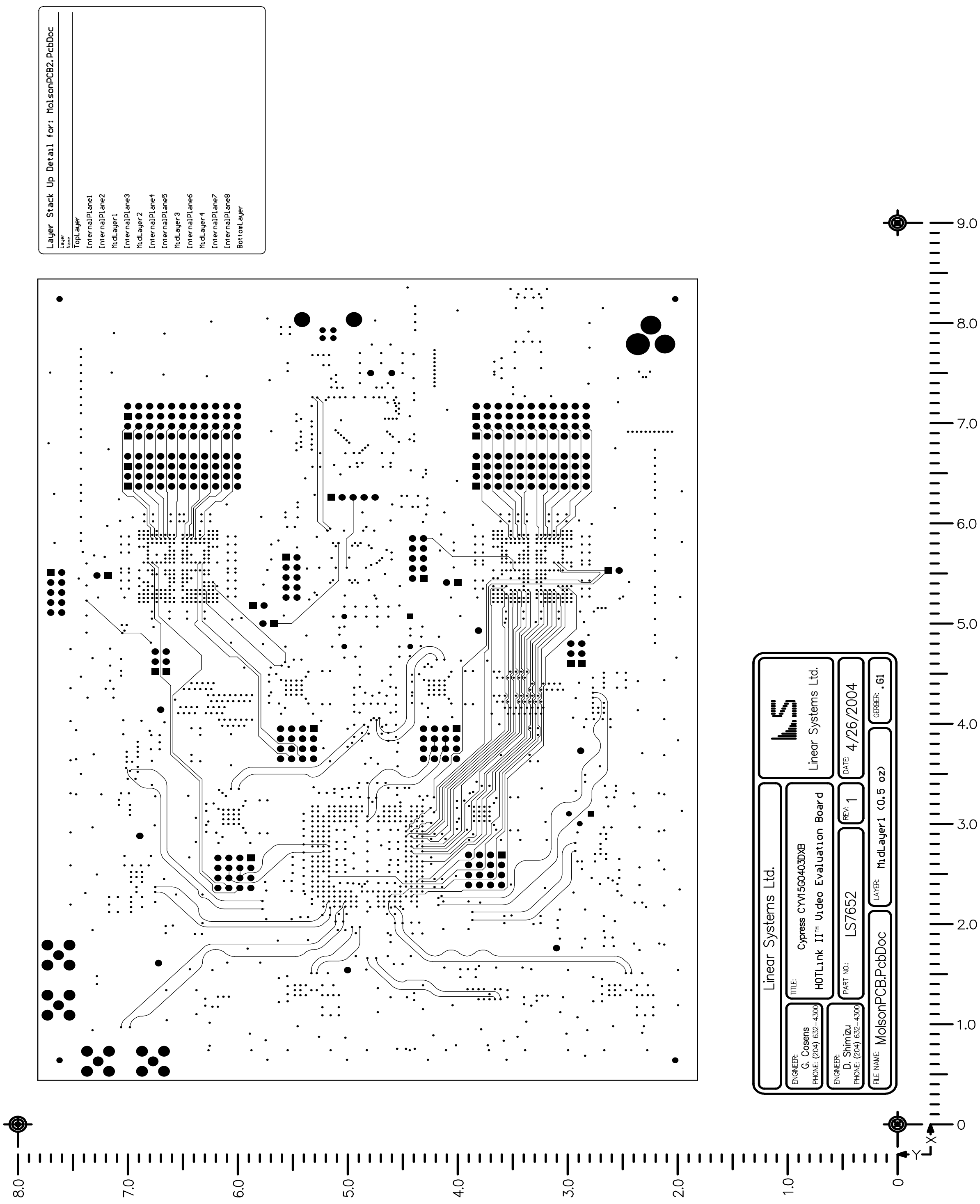


Figure B-8. Midlayer 1

[+] Feedback

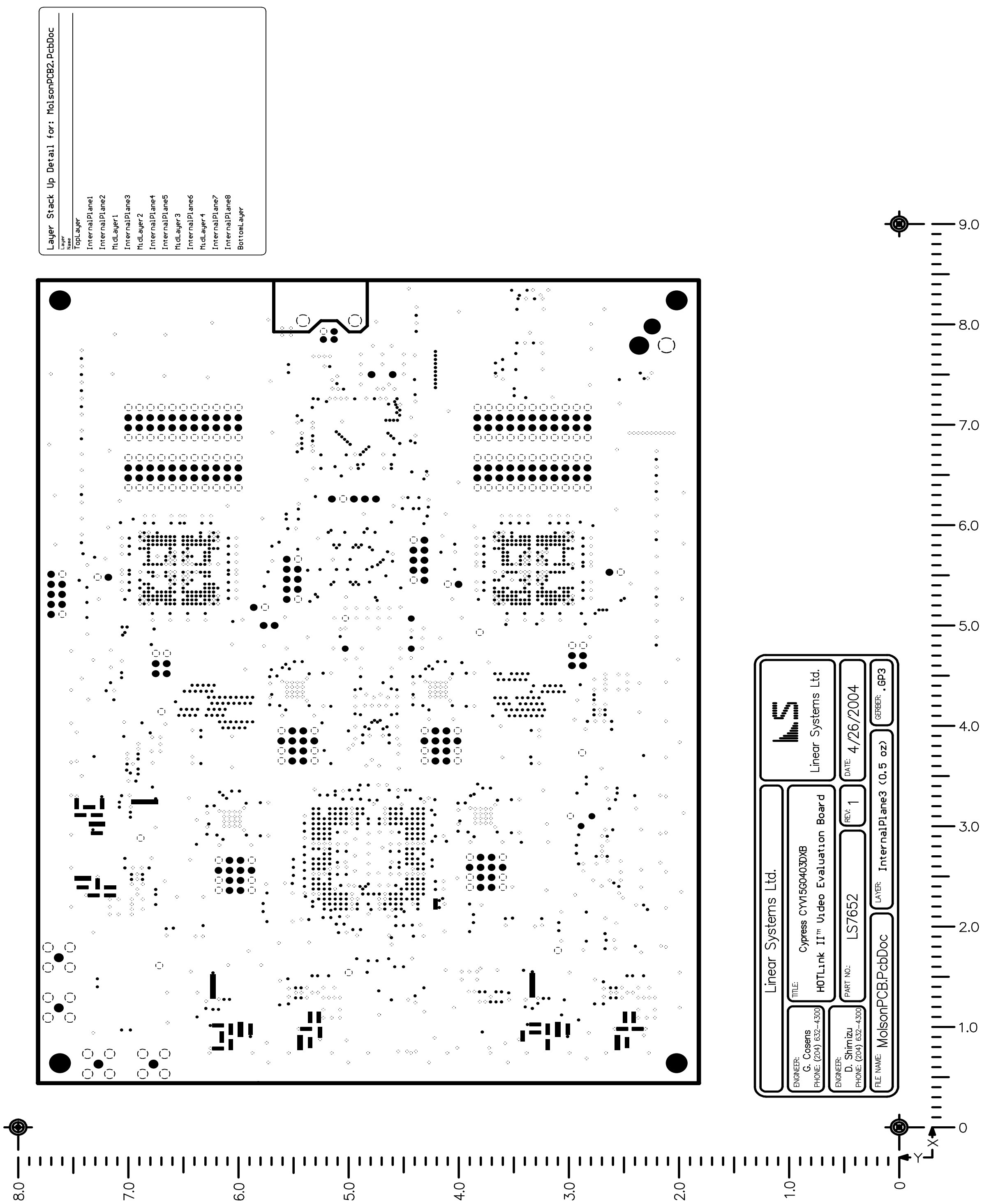


Figure B-9. Internal Plane 3

[+] Feedback

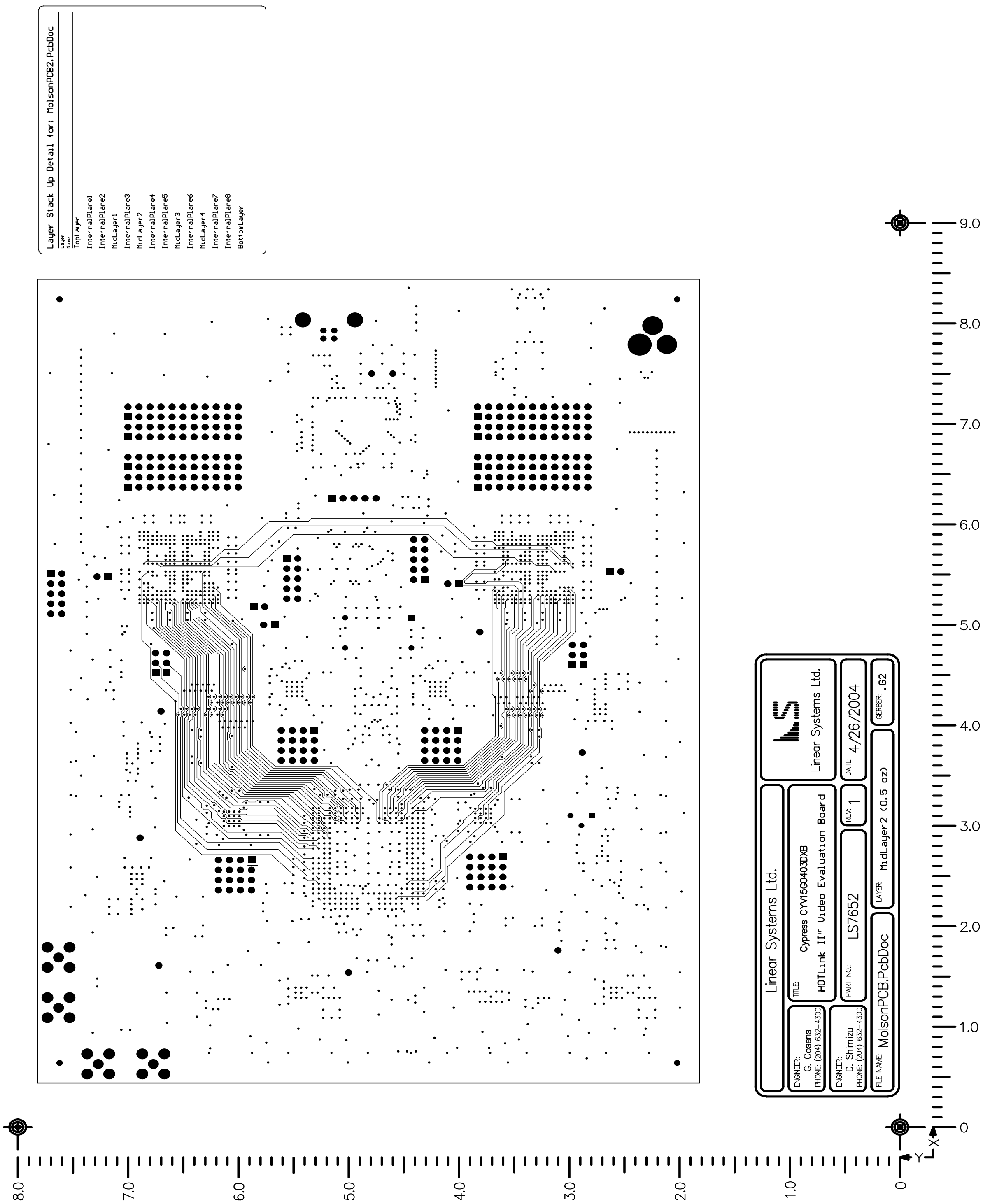


Figure B-10. Midlayer 2

[+] Feedback

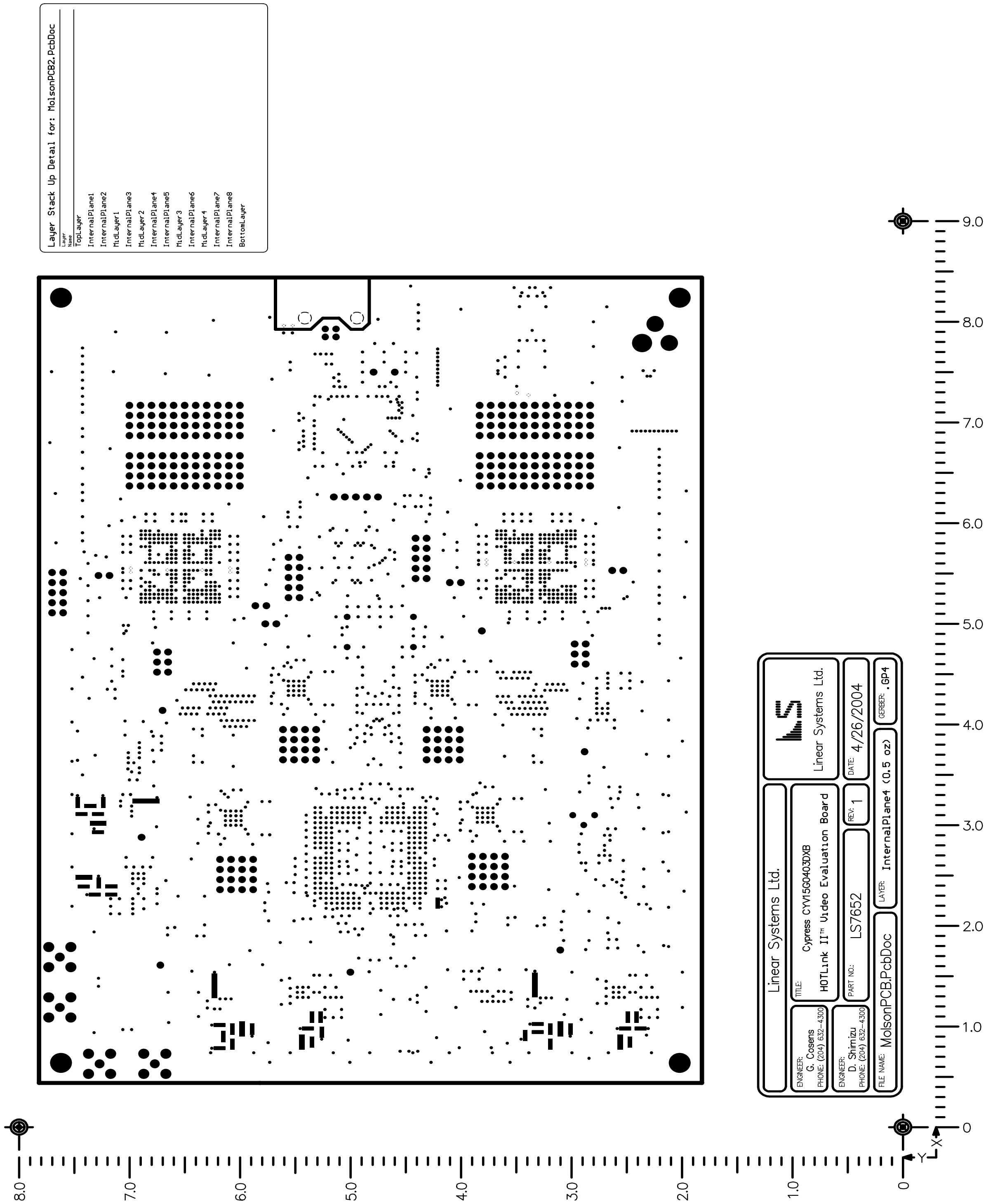


Figure B-11. Internal Plane 4

[+] Feedback

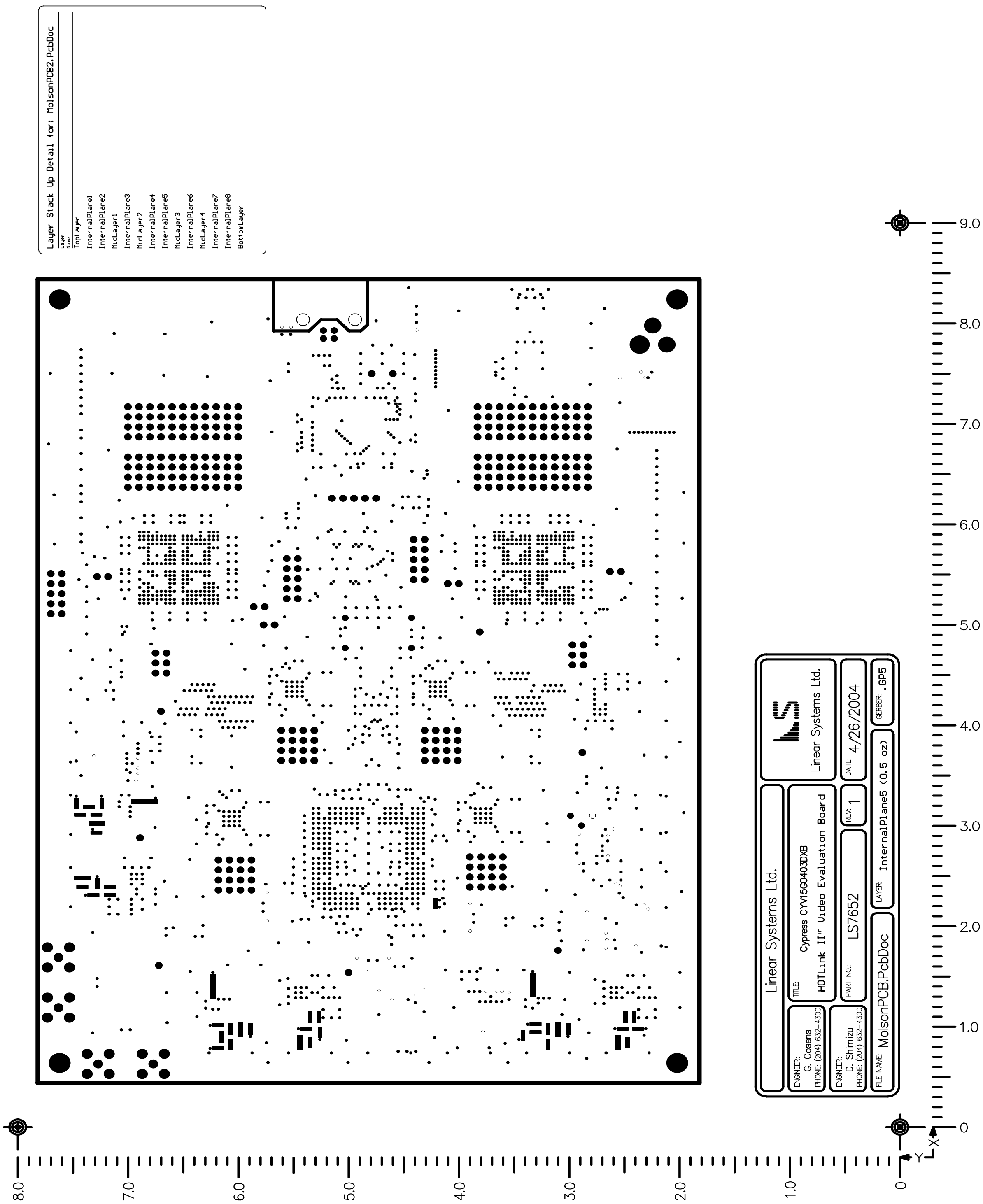


Figure B-12. Internal Plane 5

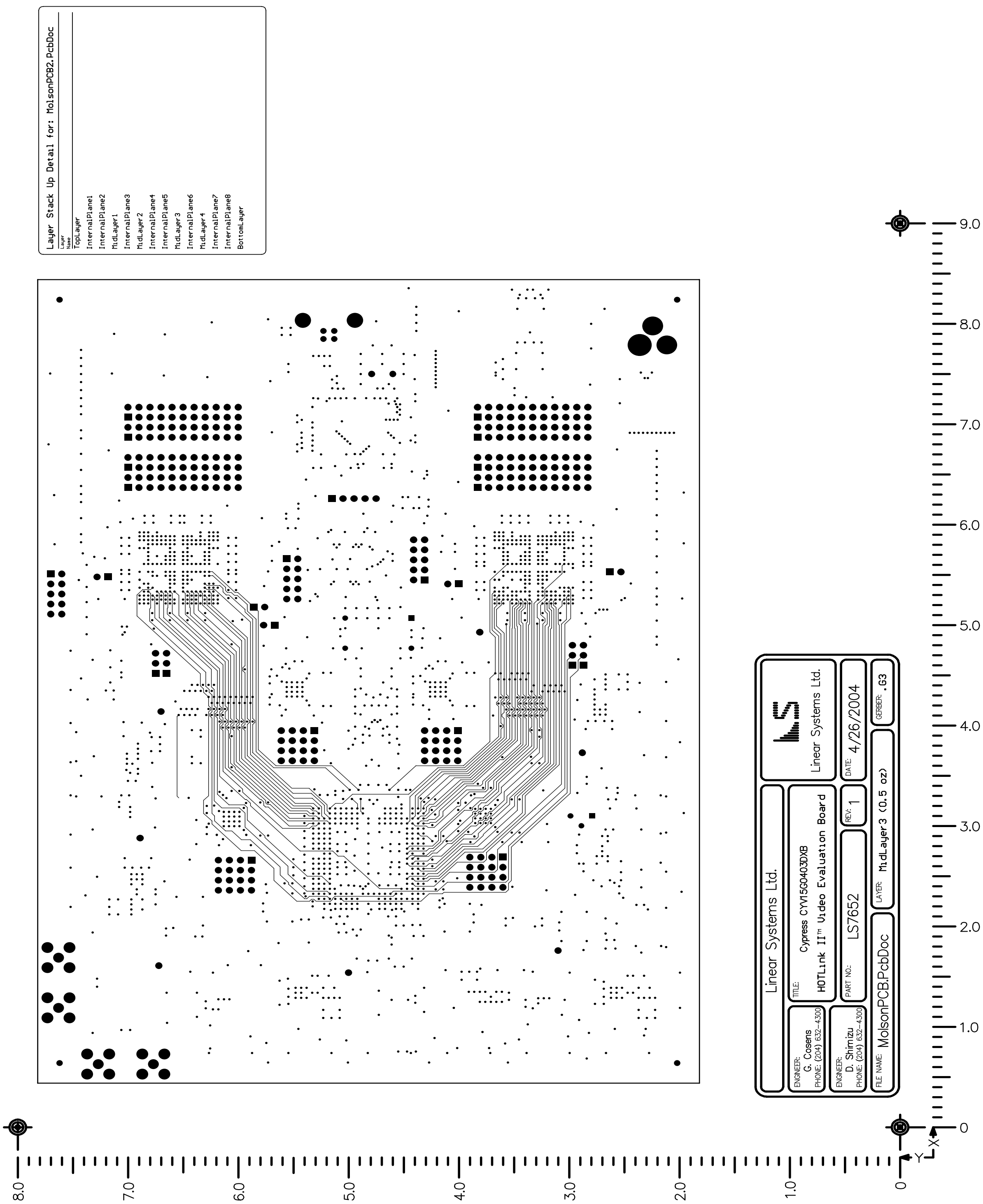


Figure B-13. Midlayer 3

[+] Feedback

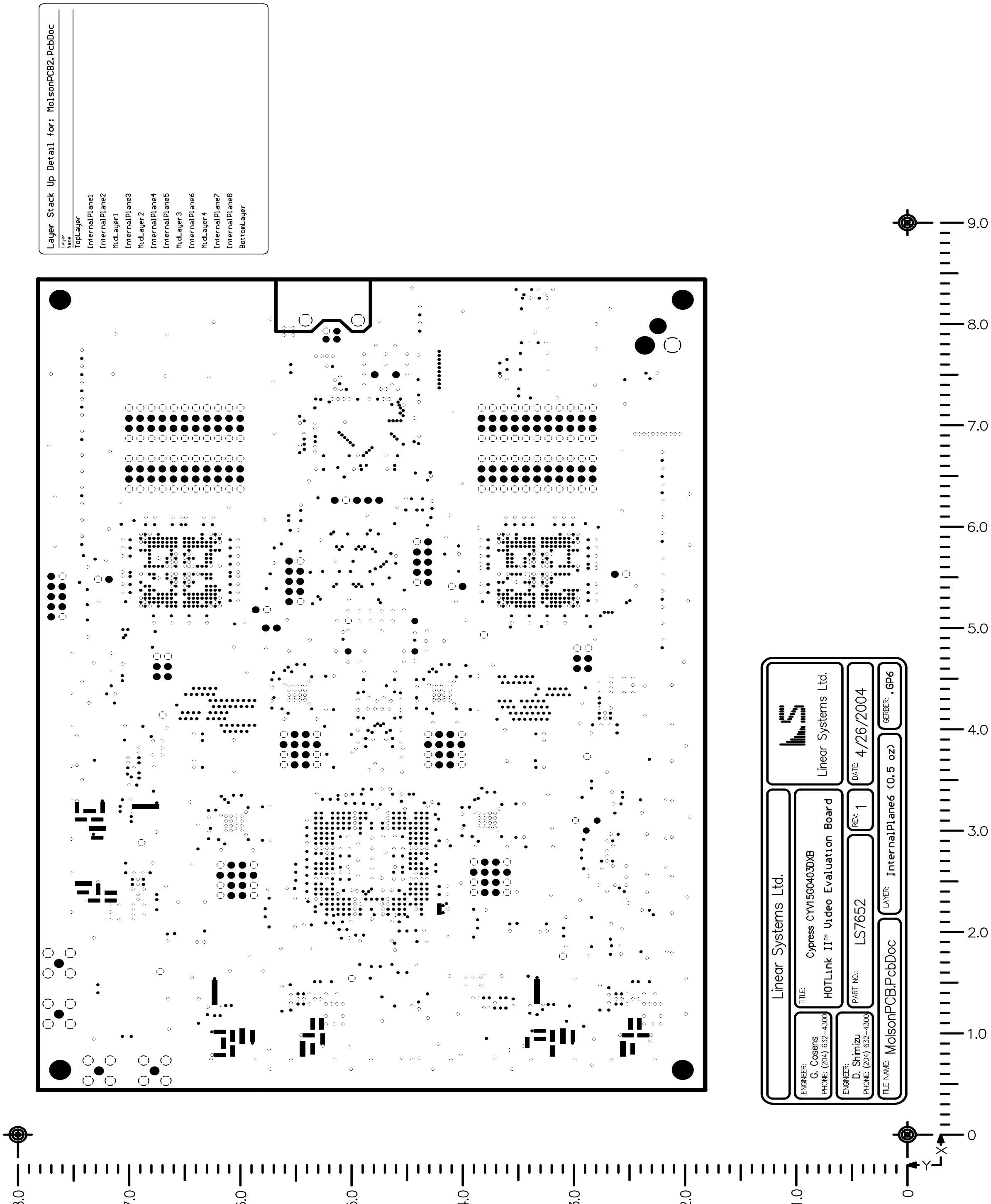


Figure B-14. Internal Plane 6

[+] Feedback

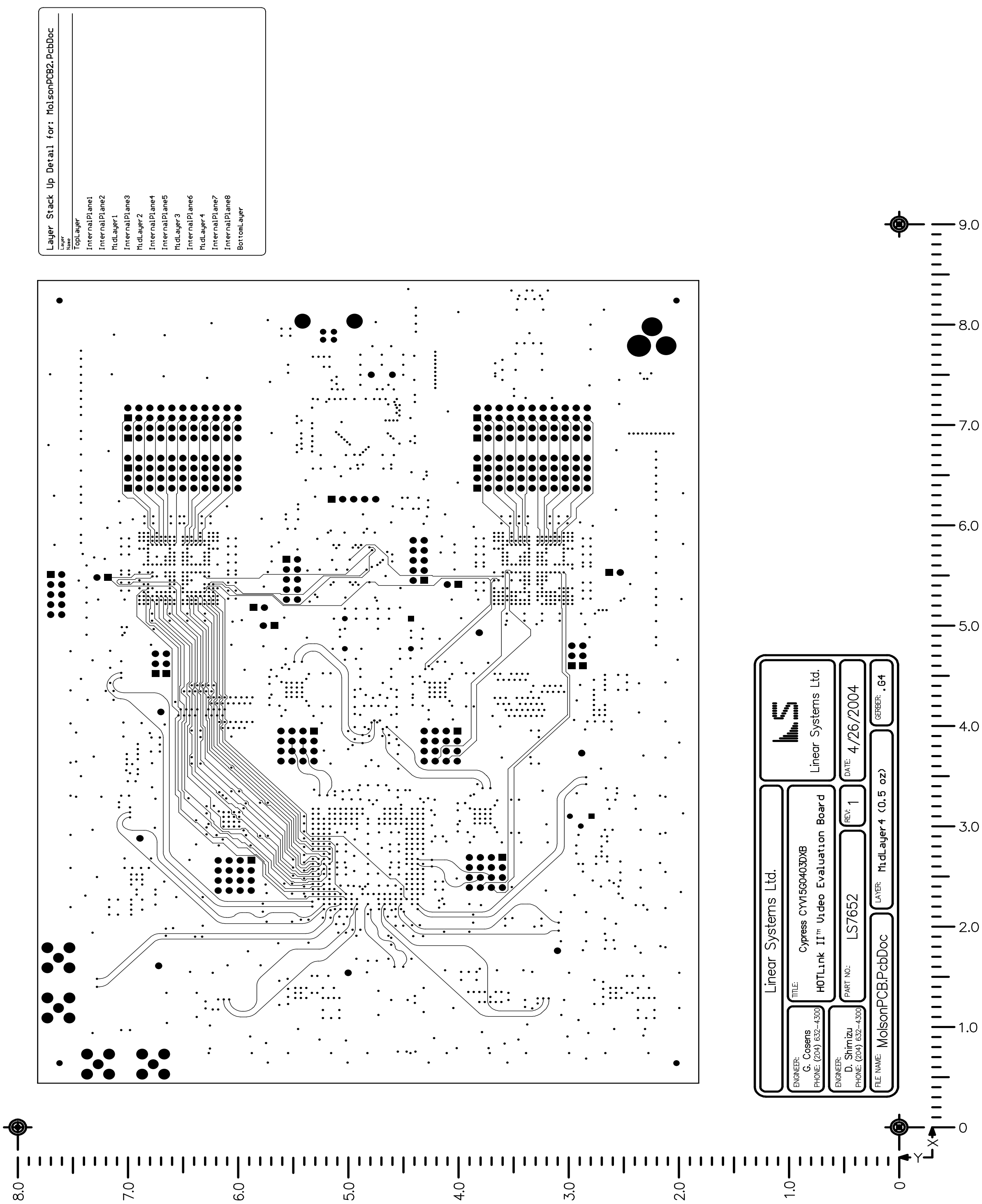


Figure B-15. Midlayer 4

[+] Feedback

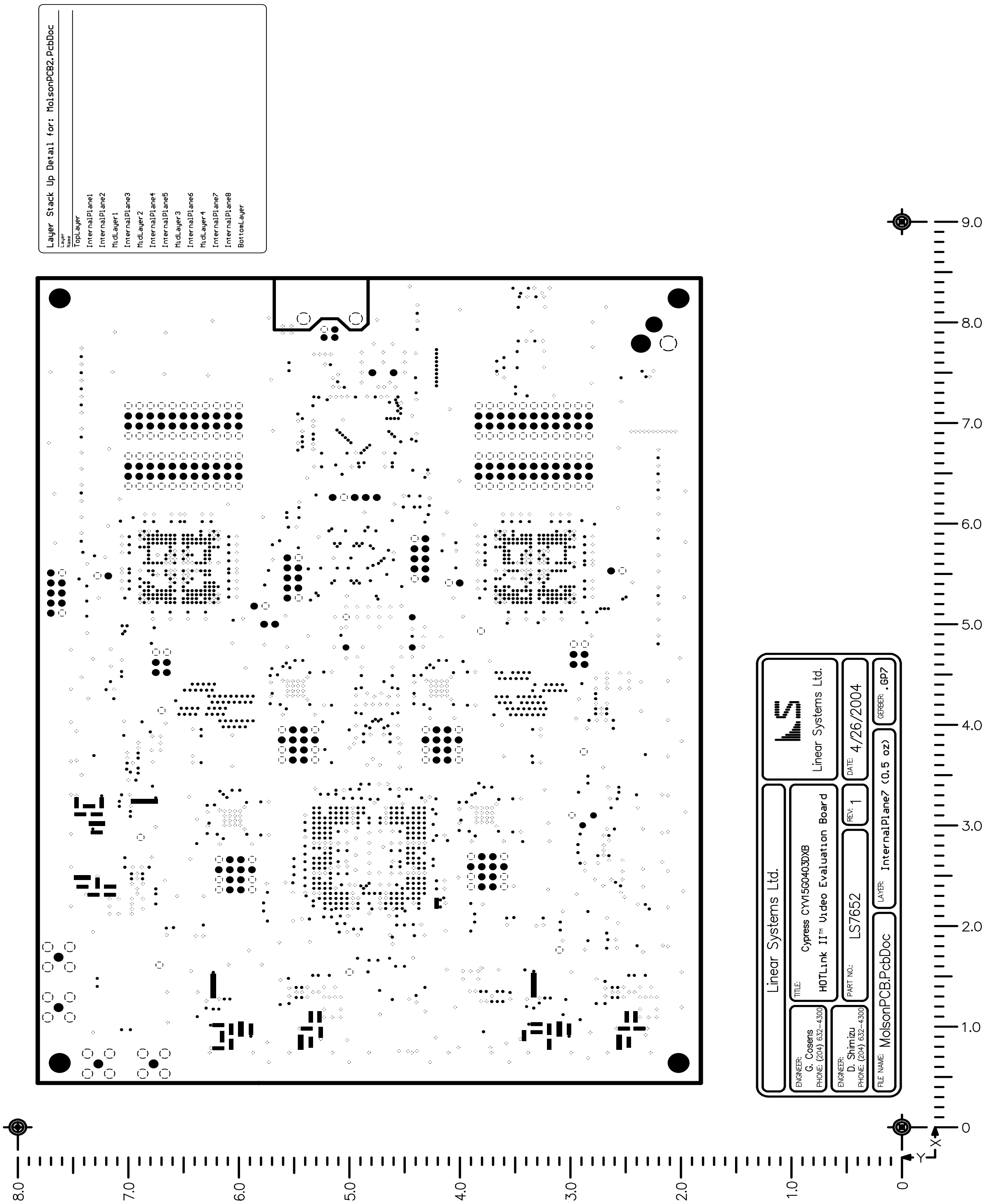


Figure B-16. Internal Plane 7

[+] Feedback

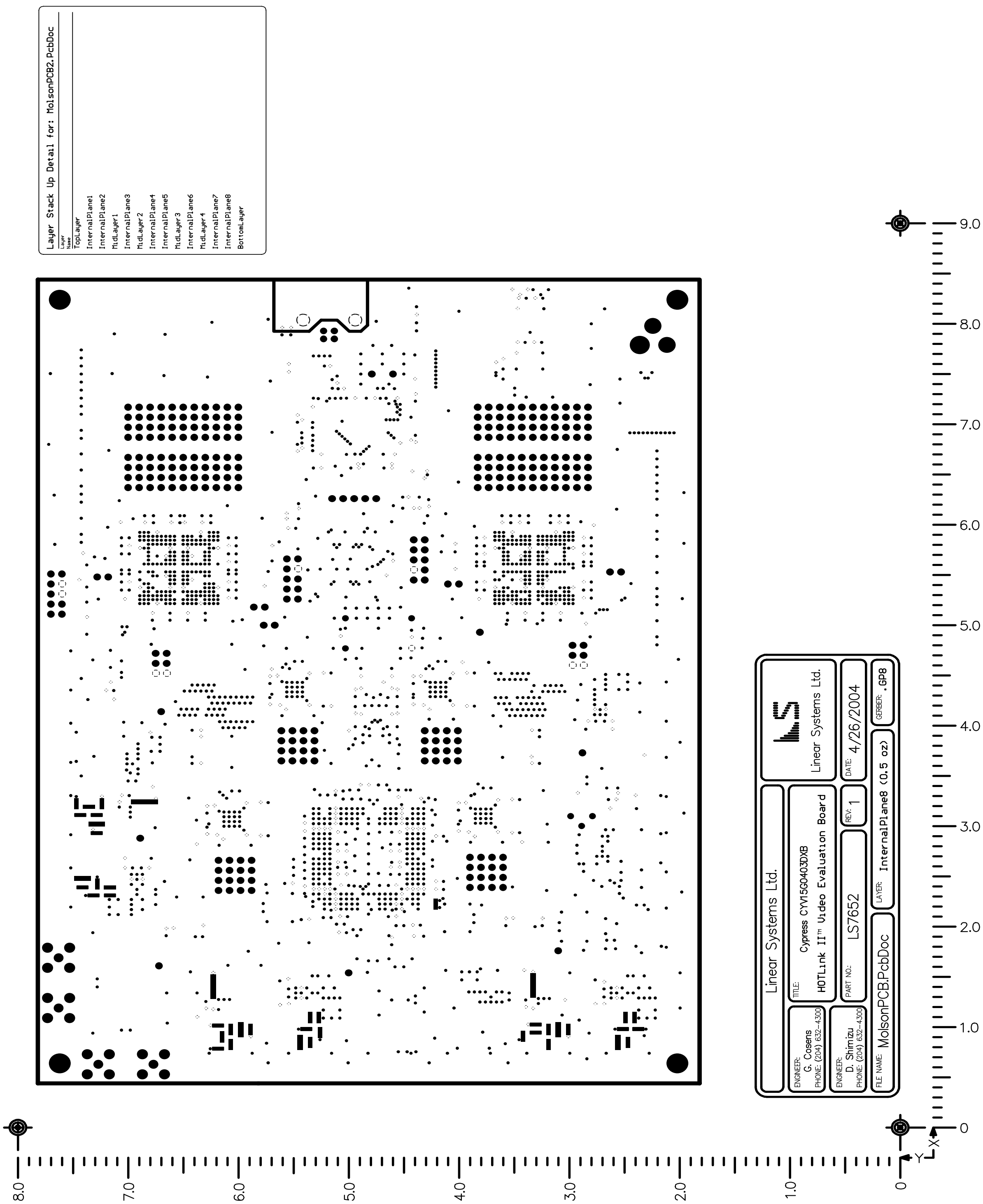


Figure B-17. Internal Plane 8

[+] Feedback

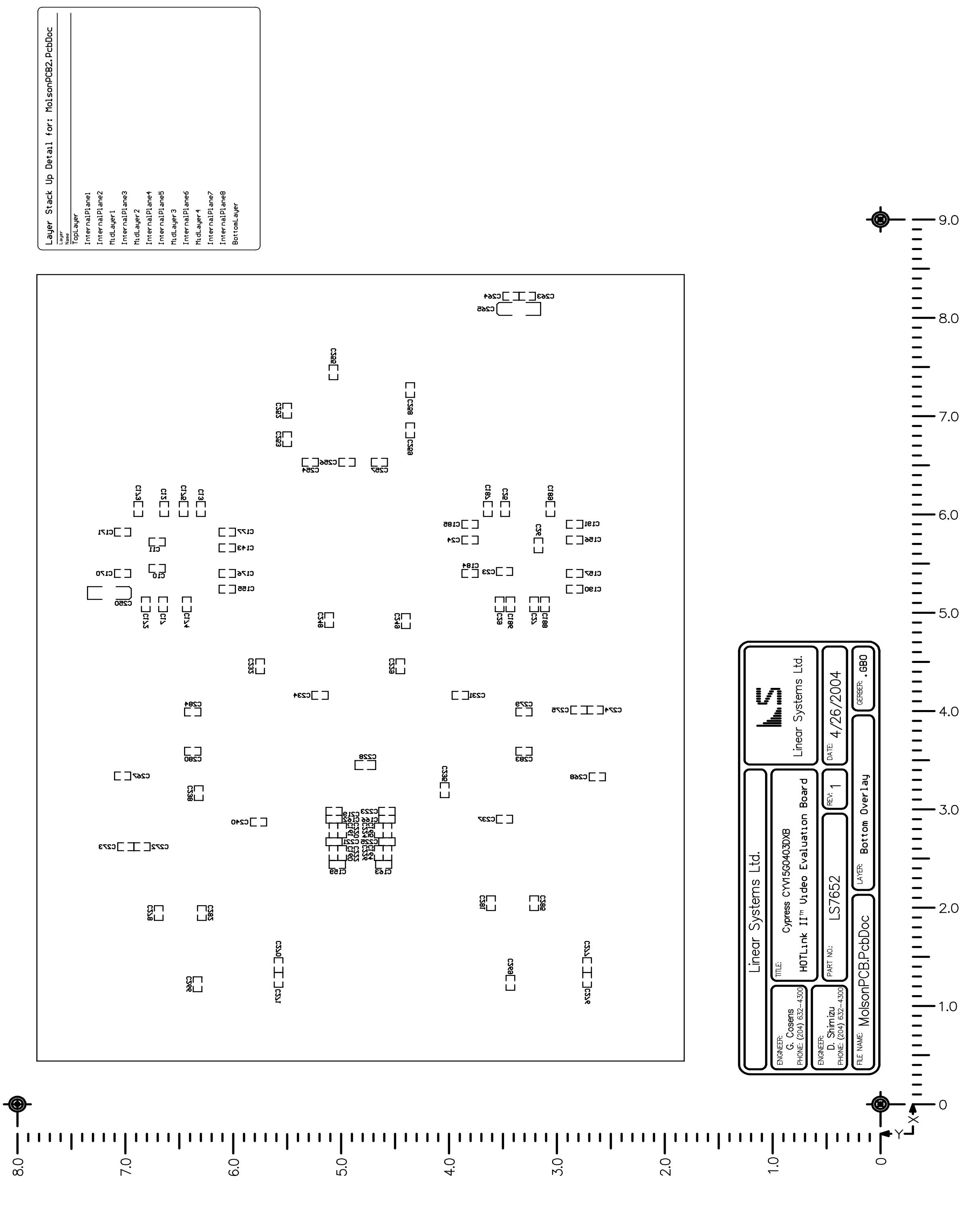


Figure B-18. Bottom Overlay

[+] Feedback

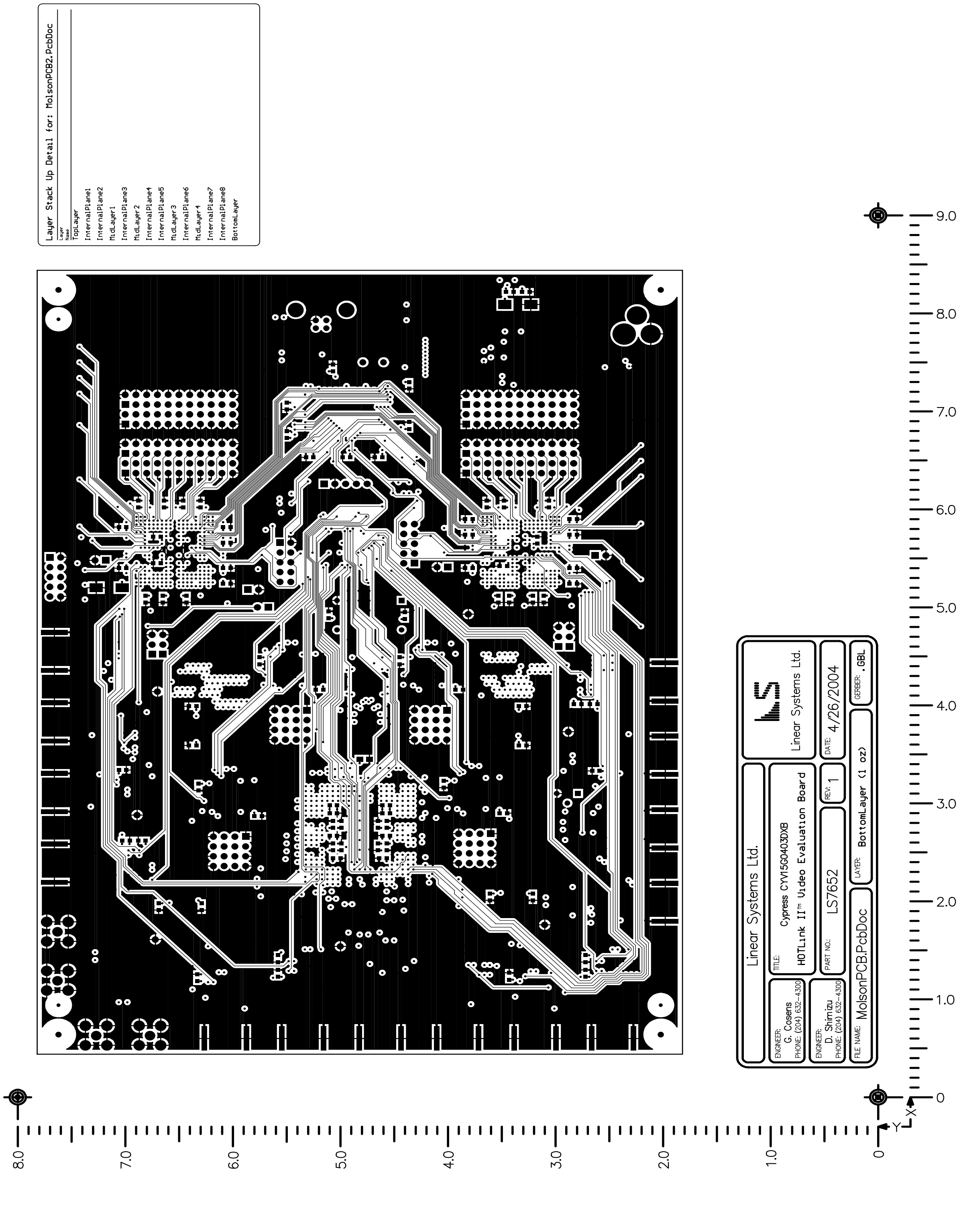


Figure B-19. Bottom Layer

[+] Feedback

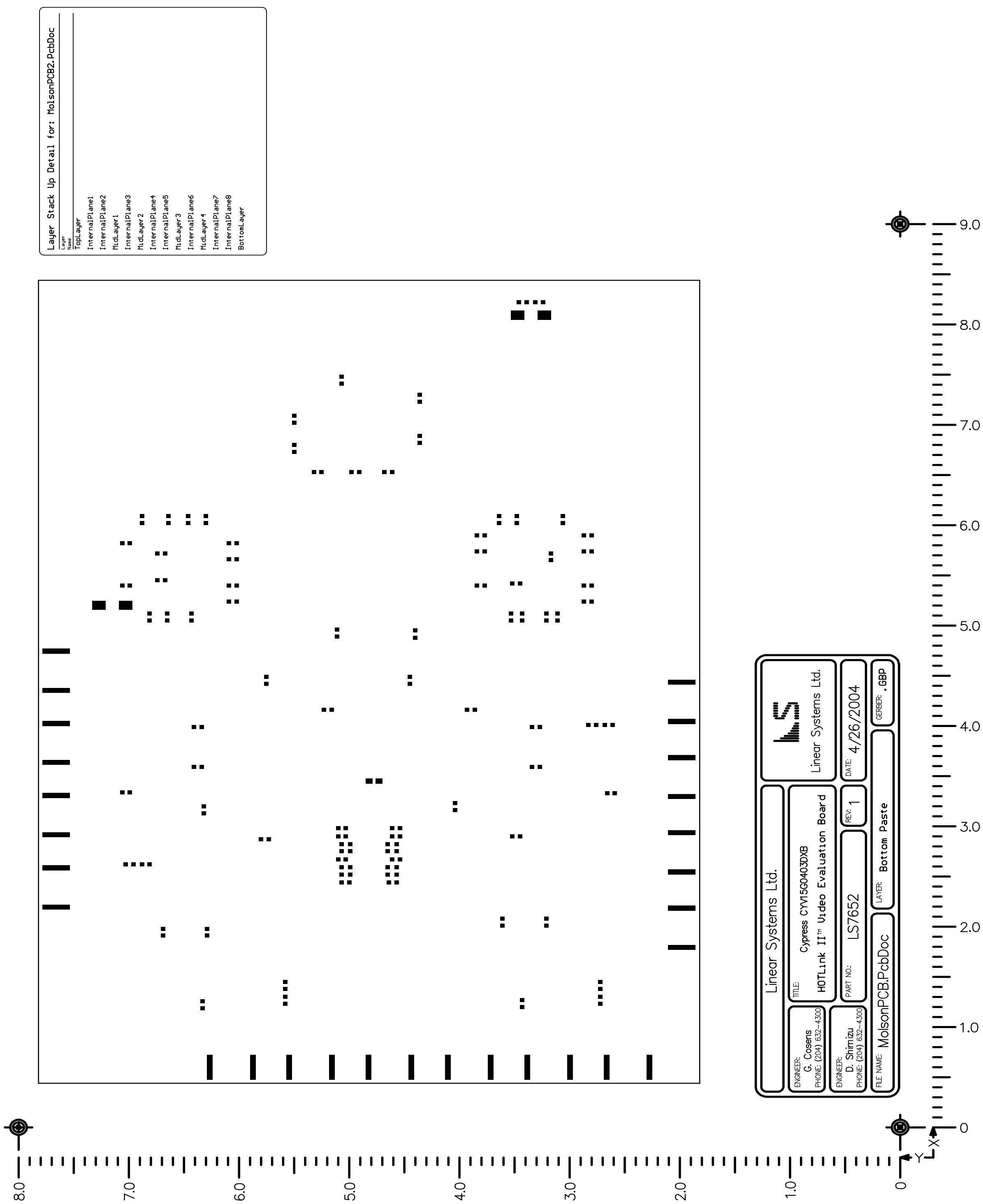


Figure B-20. Bottom Paste

[+] Feedback

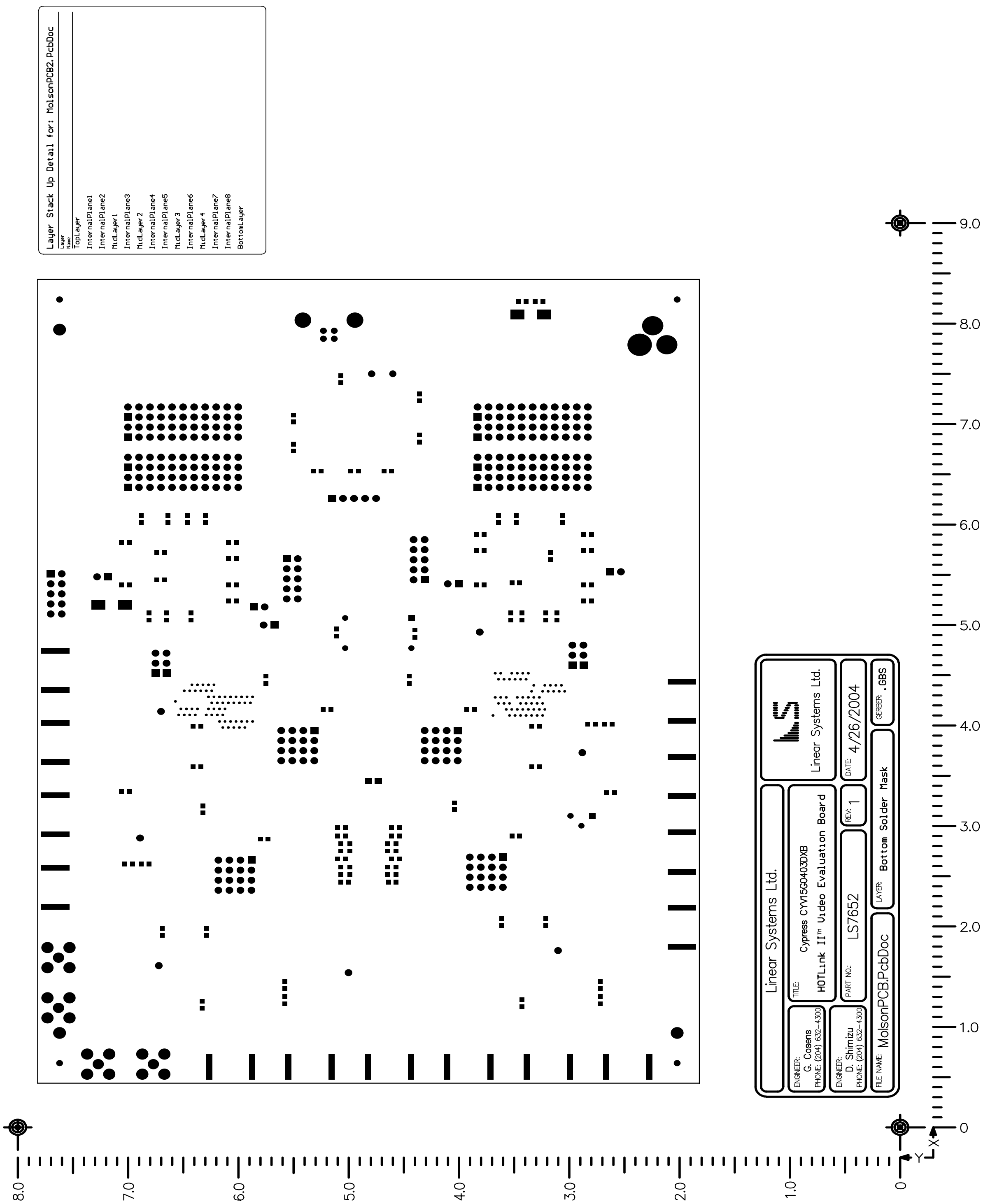


Figure B-21. Bottom Solder Mask

[+] Feedback

Appendix C: PCB Assembly Files (Drill and Assembly)

[+] Feedback

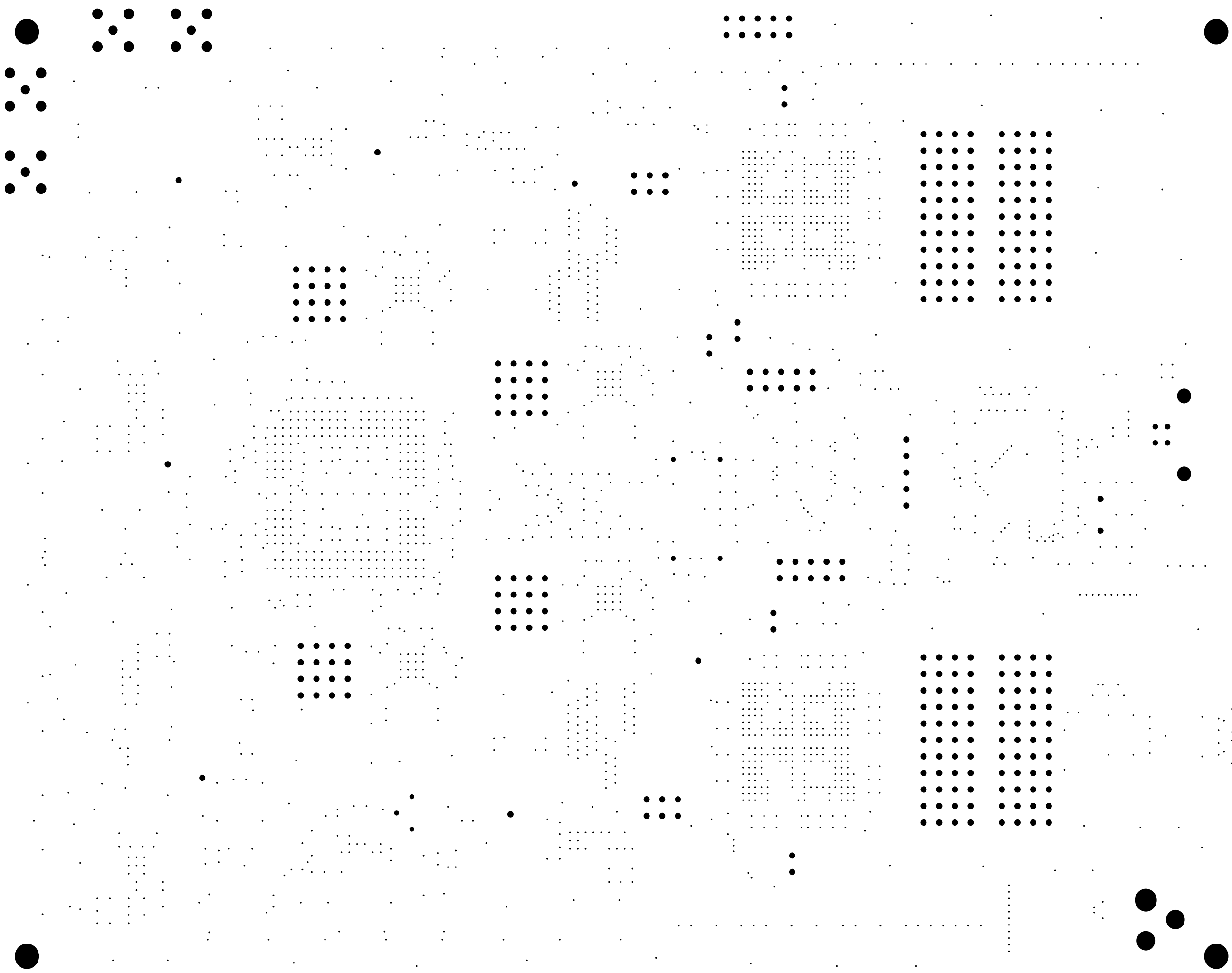


Figure C-1. Drill Placement

[+] Feedback

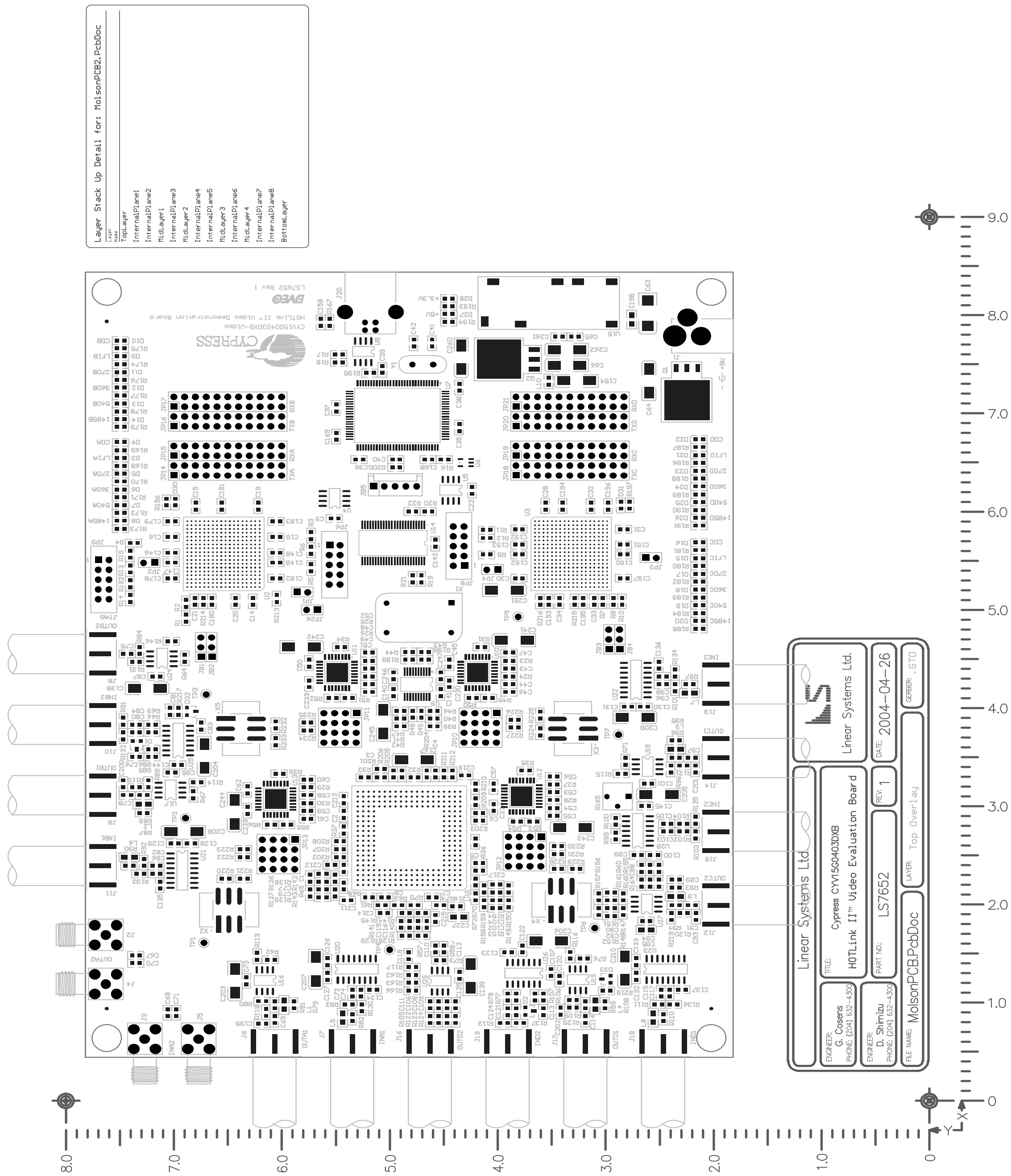


Figure C-2. Assembly–Top View

[+] Feedback

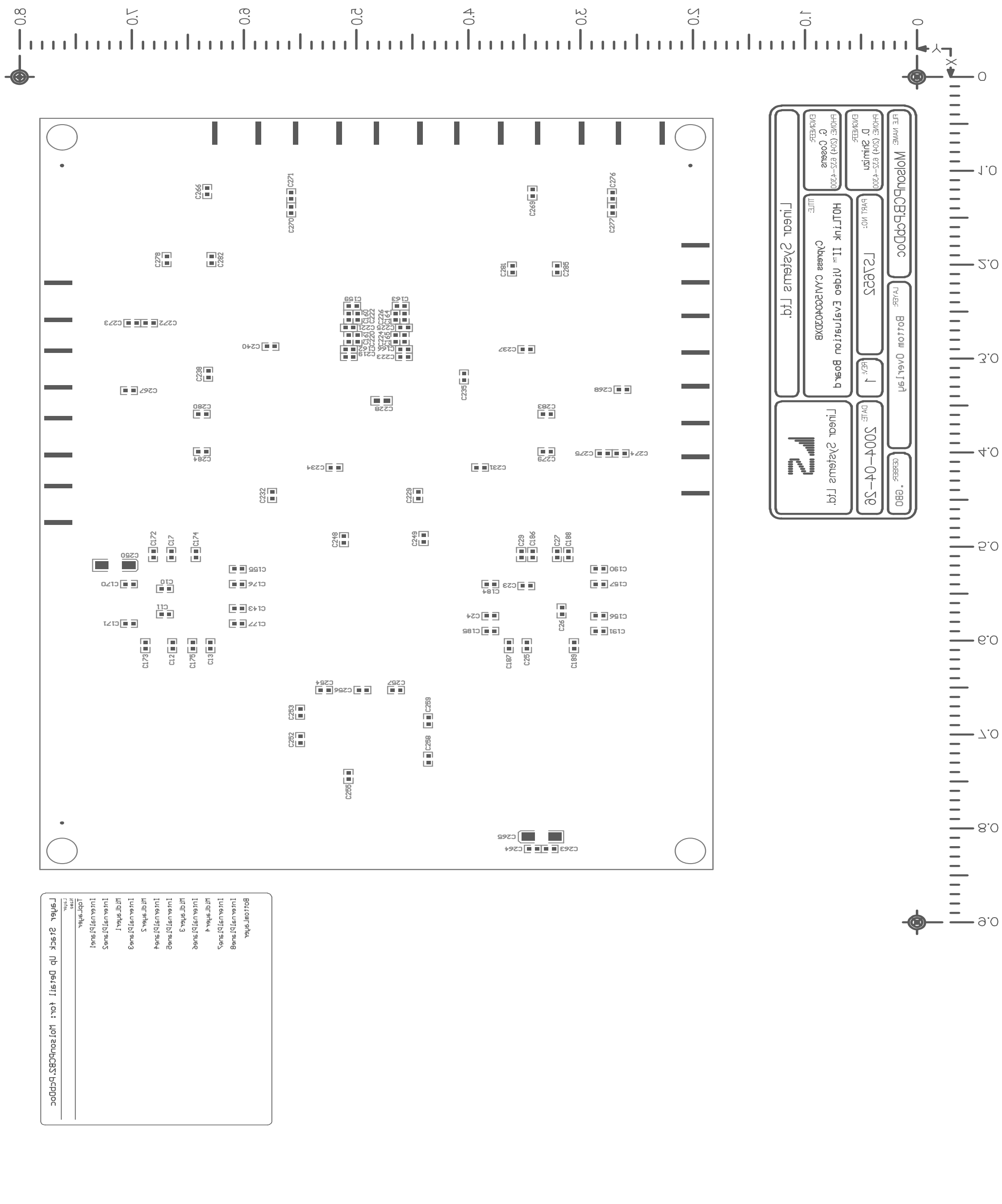


Figure C-3. Assembly–Bottom View

[+] Feedback

Appendix D: Bill of Materials (BOM) of HOTLink II CYV15G0404DXB Video Demo Board

Table D-1. Bill of Materials for HOTLink II CYV15G0404DXB Video Demo Board

Qty	Part No.	Manufacturer	Description	Designator
185	C0603C104K4RAC	Kemet	0.1-µF 10% X7R ceramic 16V 0603	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C65, C73, C81, C85, C94, C99, C100, C101, C107, C120, C122, C126, C127, C128, C129, C130, C131, C132, C133. C140, C141, C143, C144, C146, C148, C150, C152, C155, C156, C157, C159, C160, C161, C162, C163, C164, C165, C166, C168, C169, C252, C253, C254, C255, C256, C257, C258, C259, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C219, C211, C212, C213, C214, C215, C216, C217, C218, C220, C221, C222, C223, C224, C225, C226, C229,C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C246, C247, C248, C249, C261, C263, C264, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285
2	T491C685K020AS	Kemet	CAPACITOR TANT 6.8-µF 20V 10% SMD	C138, C139
4	C0603C102K5RACTU	Kemet	CAP 1000-pF 50V CERAMIC X7R 0603	C147, C149, C151, C153
1	C0603C472K5RACTU	Kemet	CAP 4700-pF 50V CERAMIC X7R 0603	C158
3	TPSC686K016R0200	AVX	CAPACITOR TANT 68-µF 20V 10% SMD	C167, C262, C265
16	T491C106K020AS	Kemet	CAPACITOR TANT 10-µF 20V 10% SMD	C203, C204, C205, C206, C207, C208, C209, C210, C241, C242, C243, C244, C245, C250, C251, C260
2	ECJ-1VC1H220J	Panasonic	22-pF 5% NPO ceramic 50V 0603	C41, C42
1	T491D107M016AS	Kemet	100-µF Tantalum 16V 7343	C63
3	T491C226K016AS	Kemet	22-µF 10% Tantalum 16V 6032	C64, C66, C154
4	C0805C105K4RAC		CAP CERAMIC 1.0-µF 16V X7R 0805	C95, C198, C227, C228

[+] Feedback

Table D-1. Bill of Materials for HOTLink II CYV15G0404DXB Video Demo Board (continued)

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9	C0603C103K5RAC	Kemet	10-nF (0.01-µF) 10% X7R ceramic 50V	C76, C87, C88, C89, C113, C118, C125, C142, C145
2	C0805C101K5GACTU	Kemet	100-pF 0805 SMT Ceramic Cap	C83, C123
4	C0603C105K8PACTU	Kemet	CAP CERAMIC 1.0-µF 10V X5R 0603	C134, C135, C136, C137
2	MMBD914	Fairchild Semiconductor	High Conductance Ultra Fast Diode	D1, D2
28	SML-LX0603GW-TR	Lumex	Surface Mount LED, Half-Moon Solder Terminals	D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D30, D31
2	SDM40E20LS	Diodes Inc.	Schottky Barrier Diode	D32, D33
1	RAPC722	Switchcraft	Conn Power Jack Right Angle PCB 2.1 mm	J1
4	142-0701-301	Johnson Components	Right angle SMA jack	J2, J3, J4, J5
1	787780-1	AMP	Universal Serial Bus Type B Receptacle	J20
14	UCBBJE20-3	Trompeter	Circuit Board Bulkhead Edge Mount Coax BNC Style Receptacle	J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19
4 * 0.075	36-140G-0	Mode	3X1 PIN	JB1, JB2, JB3, JB4
1	640456-5	AMP	5X1 PIN FRICTION LOCK	JB5
5 * 0.025	36-280G-0	Mode	HEADER 1X2	JP1, JP2, JP3, JP4, JP26
8 * 0.1	36-280G-0	Mode	HEADER 4X4 (2 X 2X4)	JP10, JP11, JP12, JP13
8	90059-0009	Molex	0.1-inch shunt, 15µ gold plate	JP10, JP11, JP12, JP13
8 * 0.275	36-280G-0	Mode	HEADER 11X2	JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21
3 * 0.125	36-280G-0	Mode	HEADER 5X2	JP6, JP8, JP9
4	LL2012-F5N6K	Toko America	5.6-nH 0805 Inductor	L1, L2, L3, L4
1	BLM18BD102SN1D	Murata	FERRITE CHIP 1000-OHM 100-MA 0603	L10
4	LL2012-F10NK	Toko America	10-nH 0805 Inductor	L5, L6, L7, L8
1	LL2012-F8N2K	Toko America	8.2-nH 0805 Inductor	L9
1	LM2940CS-5.0	National Semiconductor	3-Terminal Positive Regulator	Q1
1	LT1587CM-1.5		3-Terminal Positive Regulator	Q2

[+] Feedback

Table D-1. Bill of Materials for HOTLink II CYV15G0404DXB Video Demo Board (continued)

Qty	Part No.	Manufacturer	Description	Designator
21	ERJ-3GEY0R00V	Panasonic	RES ZERO-OHM 1/10W 5% 0603 SMD	R1, R2, R7, R8, R19, R20, R21, R22, R192, R213, R214, R215, R216, R222, R223, R226, R227, R230, R231, R234, R235
5	ERJ-3GEYJ751V	Panasonic	RES 750-OHM 1/10W 5% 0603 SMD	R113, R114, R115, R116, R117
8	ERJ-3GEYJ151V	Panasonic	RES 150-OHM 1/10W 5% 0603 SMD	R118, R119, R120, R121, R122, R123, R124, R125
5	ERJ-3GEYJ102V	Panasonic	RES 1.0K-OHM 1/10W 5% 0603 SMD	R13, R14, R15, R195, R200
8	ERJ-3EKF37R4V	Panasonic	RES 37.4-OHM 1/16W 1% 0603 SMD	R130, R131, R132, R133, R134, R135, R136, R137
1	ERJ-3EKF1911V	Panasonic	RES 1.91K-OHM 1/16W 1% 0603 SMD	R146
1	ERJ-3GEYJ681V	Panasonic	RES 680-OHM 1/10W 5% 0603 SMD	R155
1	ERJ-3GEYJ472V	Panasonic	RES 4.7K-OHM 1/10W 5% 0603 SMD	R16
4	ERJ-3EKF51R1V	Panasonic	RES 51.1-OHM 1/16W 1% 0603 SMD	R160, R161, R162, R163
1	ERJ-3EKF59R0V	Panasonic	RES 59.0-OHM 1/16W 1% 0603 SMD	R164
1	CT6W104	BC Components	POT 100K 6-MM CERM SQ ST TOP	R165
1	ERJ-3EKF1541V	Panasonic	RES 1.54K-OHM 1/16W 1% 0603 SMD	R166
1	ERJ-3GEYJ105V	Panasonic	RES 1.0M-OHM 1/10W 5% 0603 SMD	R167
27	9C06031A2210FKHFT	Yageo America	RES 221-OHM 1/10W 1% 0603 SMD	R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R193, R196, R197
2	ERJ-3GEYJ222V	Panasonic	RES 2.2K-OHM 1/10W 5% 0603 SMD	R17, R18
1	ERJ-3GEYJ361V	Panasonic	RES 360-OHM 1/10W 5% 0603 SMD	R194
10	ERJ-3EKF1300V	Panasonic	RES 130-OHM 1/16W 1% 0603 SMD	R198, R199, R220, R221, R224, R225, R228, R229, R232, R233
4	ERJ-3EKF10R0V	Panasonic	RES 10.0-OHM 1/16W 1% 0603 SMD	R201, R202, R203, R204
8	9C06031A22R0FKHT	Yageo America	RES 22.0-OHM 1/10W 1% 0603 SMD	R205, R206, R207, R208, R209, R210, R211, R212
9	ERJ-3GEYJ202V	Panasonic	RES 2.0K-OHM 1/10W 5% 0603 SMD	R23, R24, R25, R26, R27, R28, R29, R30, R60
8	ERJ-3GEYJ103V	Panasonic	RES 10K-OHM 1/10W 5% 0603 SMD	R3, R4, R5, R6, R9, R10, R11, R12
26	ERJ-3GEYJ101V	Panasonic	RES 100-OHM 1/10W 5% 0603 SMD	R31, R32, R33, R34, R35, R36, R37, R38, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78
8	ERJ-3EKF1470V	Panasonic	RES 147-OHM 1/16W 1% 0603 SMD	R39, R40, R41, R42, R45, R46, R47, R48
4	ERJ-3GEYJ820V	Panasonic	RES 82-OHM 1/10W 5% 0603 SMD	R43, R44, R217, R218
8	ERJ-3EKF1210V	Panasonic	RES 121-OHM 1/16W 1% 0603 SMD	R49, R50, R51, R52, R53, R54, R55, R56

Table D-1. Bill of Materials for HOTLink II CYV15G0404DXB Video Demo Board (continued)

Qty	Part No.	Manufacturer	Description	Designator
36	ERJ-3EKF75R0V	Panasonic	RES 75.0-OHM 1/16W 1% 0603 SMD	R59, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R219
1	CYV15G0404DXB-BGC	Cypress	Independent Clock Quad HOTLink II Transceiver	U1
4	SY87729LHI	Micrel	3.3V AnyClock Fractional N Synthesizer	U10, U11, U12, U13
1	CY8C27643-24PVI	Cypress	PSoC Mixed Signal Array	U14
1	APC08F08	Astec	CONV DC-DC 25W 8VIN 3.3VOUT SMD	U15
2	EP1C20F324C8	Altera	Cyclone FPGA	U2, U3
4	GS1528-CKA	Gennum	HD-LINX II Multi-Rate SDI Dual Slew-Rate Cable Driver	U16, U17, U18, U19
4	GS1524-CKD	Gennum	HD-LINX II Multi-Rate SDI Adaptive Cable Equalizer	U20, U21, U22, U23
1	CLC001AJE	National Semiconductor	Serial Digital Cable Driver with Adjustable Outputs	U24
2	CLC014AJE	National Semiconductor	Adaptive Cable Equalizer for High-Speed Data Recovery	U25, U26
1	GS9028-CKA	Gennum	GENLINX II Cable Driver with Two Adjustable Outputs	U27
1	GS9024-CKB	Gennum	GENLINX II Automatic Cable Equalizer	U28
1	CLC007AJE	National Semiconductor	Serial Digital Cable Driver with Dual Complementary Outputs	U29
2	EPCS4SI8	Altera	Configuration device	U4, U5
1	TPS3820-33	TI	Processor Supervisory Circuit	U6
1	CY7C68013-100AC	Cypress	EZ-USB FX2 USB Microcontroller High-Speed USB Peripheral Controller	U7
1	24LC00/SN	Microchip	128-bit I2C Bus Serial EEPROM(SOIC)	U8
1	CY2DP314OI	Cypress	1 of 2:4 Differential Fanout Buffer	U9
1	SEL2431A-27.0000MHz PE1144MV-27.0M	Saronix Pletronics	27-MHz PECL OSCILLATOR MODULE	X1
4	VF261-SL-74.25 MHz XO-500-DFC-205N-74.25 MHz	Valpey Fisher Vectron	74.25-MHz SMT OSCILLATOR +/- 20ppm	X2, X3, X4, X5
1	ECS-240-20-4	ECS	24-MHz 20-pF load Crystal	Y1
4			6-32 threaded Nylon standoffs	
4			6-32 Nylon screws	
1	LS7652 Rev 2		14 Layer PCB	
1	DTS060330UDC-P5P	CUI Inc.	Universal input 6V 20W power supply, 2.1-mm center-positive plug	
1	P012-006	Tripp Lite	NEMA 1-15P to IEC 320 C7 power cable, 6'	

[+] Feedback

Table D-1. Bill of Materials for HOTLink II CYV15G0404DXB Video Demo Board (continued)

Qty	Part No.	Manufacturer	Description	Designator
			Do not populate	R57, R58, R126, R127, R128, R129, R138, R139, R140, R141, R142, R143, R144, R145, R147, R148, R149, R150, R151, R152, R153, R154, R156, R157, R158, R159

[+] Feedback

Appendix E: Unpacking HOTLink II CYV15G0404DXB Video Demo Board

[+] Feedback

The software GUI must be installed from the resource CD included in the kit. Please follow instructions listed below for installing and running the various tests from the GUI.

HOTLink II CYV15G0404DXB Video Demo Board Software Set-up Instructions

Open the CD that was supplied with the kit and locate the file named "HOTLink II Video Demo Board Set-up.exe" located in the zip file. Follow the on screen instructions to set up the GUI. This will install the GUI for the video demo board software to run on your PC/Laptop. A Windows 2000/XP operating system environment is a minimum requirement to run the software. The following instructions on installation are based on the Windows XP operating system environment.

1. Locate the file *HOTLink II Video Demo Board set-up.exe*. Double click the icon.
2. When a dialog box pops up to confirm installation, click "Yes" to continue (see *Figure E-1*). This will launch the installation wizard.



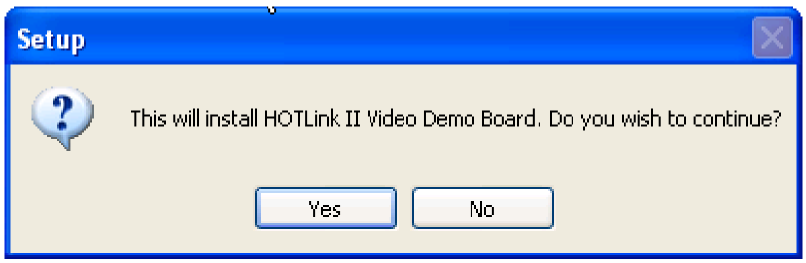


Figure E-1. Software Set-up Dialog Box

3. Click "Next" to continue.

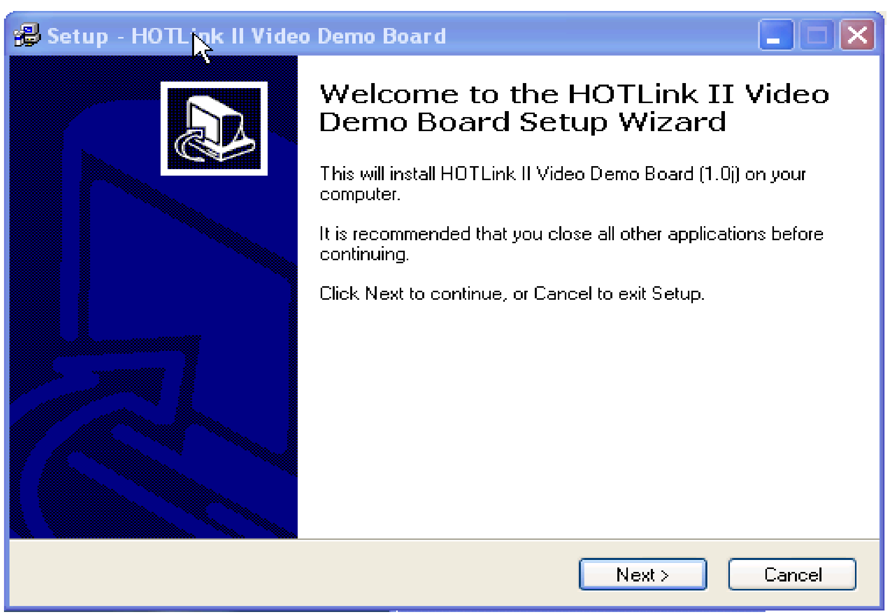


Figure E-2. Software Set-up Wizard

4. Select the folder where the HOTLink II Video Demo Board software will be installed, then click on "Next."

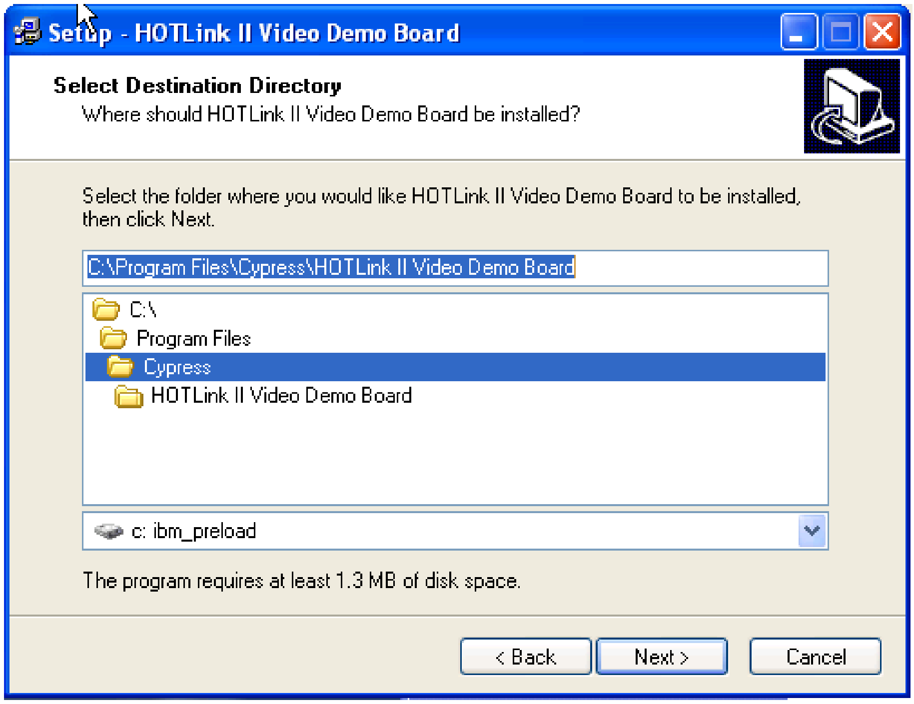


Figure E-3. Software Set-up Wizard 2

5. Select the Start menu folder in which the HOTLink II Video Demo Board shortcut will be created, then click on "Next."

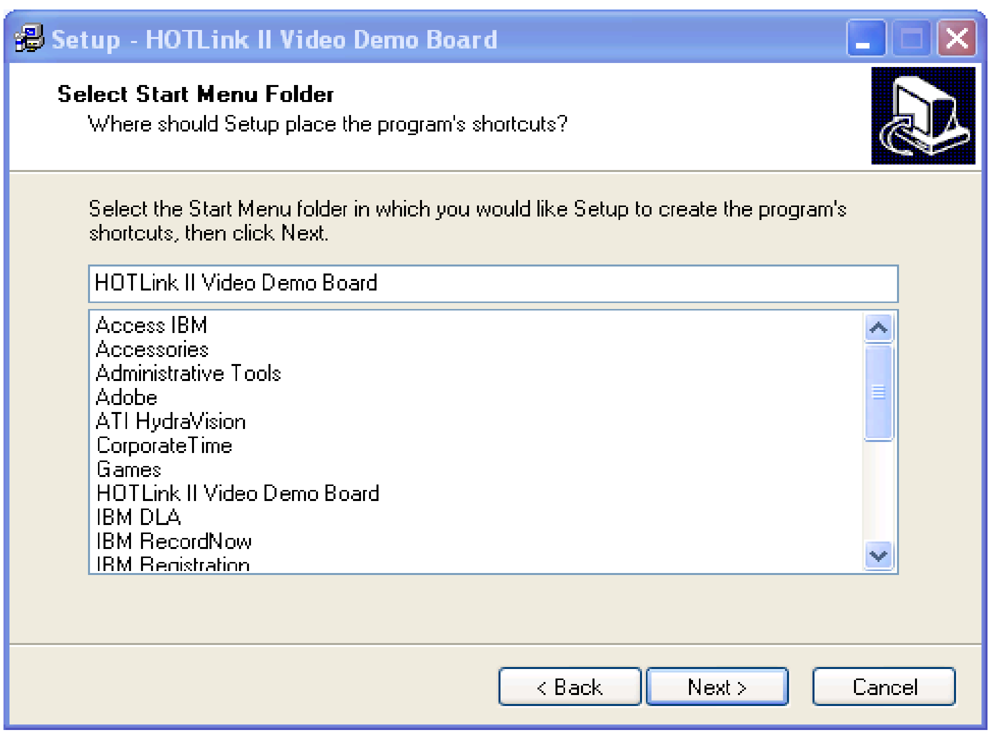


Figure E-4. Software Set-up Wizard 3

6. Click on the check box to have the software icon installed either on desktop, or as a quick launch icon, or both, then click “Next.”

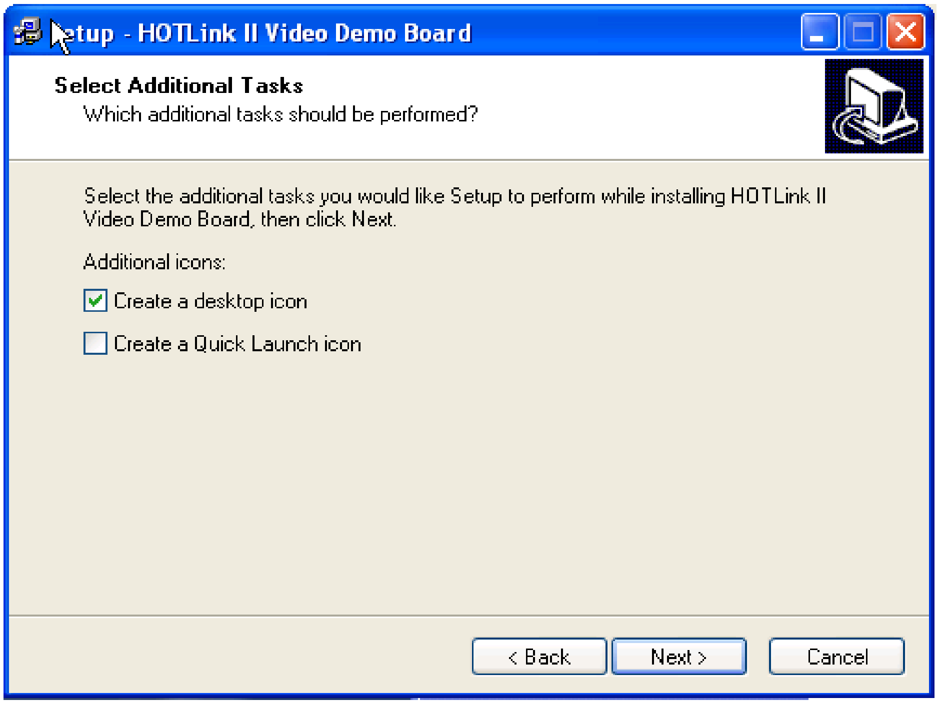


Figure E-5. Software Set-up Wizard 4

7. Click install to have the software installed.

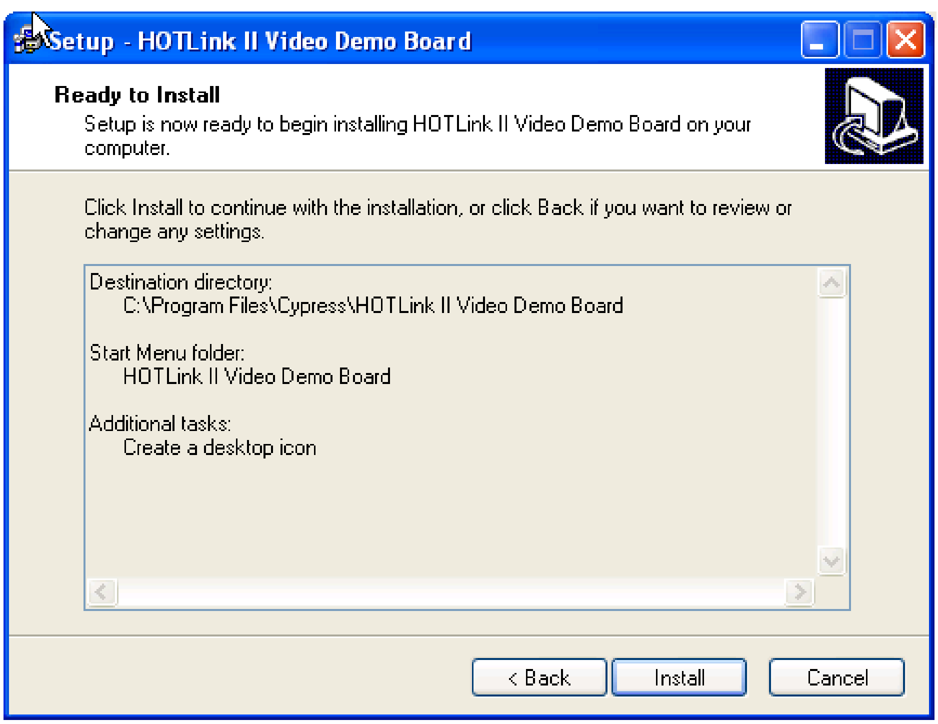


Figure E-6. Software Set-up Wizard 5

[+] Feedback

The HVDB icon will now be available on your Desktop and/or as a Quick Launch item in your taskbar (depending on your selections during installation).

Connect the 6V DC power supply to the power supply jack (J1) on the board. The power LEDs on the board will turn on.

Connect the USB cable between the USB port of the video board and the PC/laptop. Once the USB connection from PC/laptop is made, the “Found New Hardware Wizard” will pop up indicating that new hardware has been detected and the drivers may need to be installed if they are not present. See *Figure E-7*.

1. Choose “Install the software automatically (Recommended)”, then click on “Next.”



Figure E-7. New Hardware Wizard

2. If a warning window pops up as shown in *Figure E-8*, click on “Continue Anyway.”

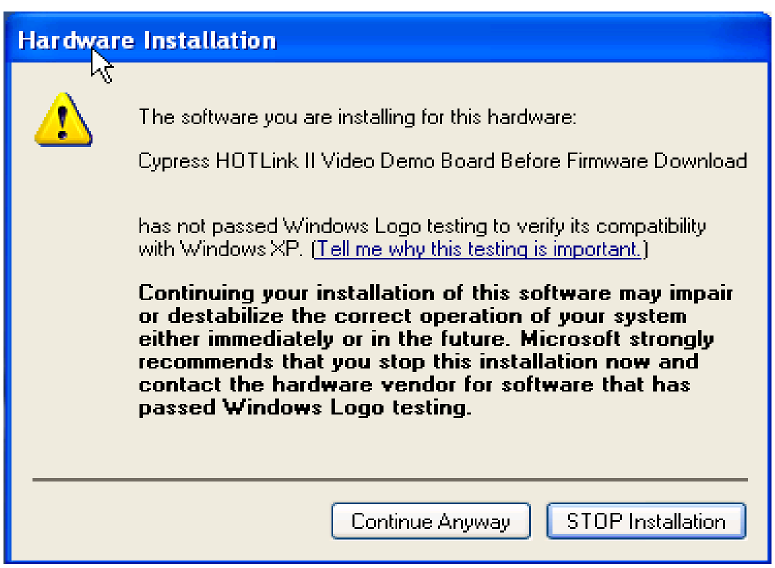


Figure E-8. Hardware Installation

[+] Feedback

3. “Completing the Find New Hardware Wizard” will pop up. Click on “Finish.”



Figure E-9. New Hardware Wizard 2

4. Click on the HVDB icon on your desktop or Quick Launch taskbar. The HVDB GUI should appear as shown in *Figure E-15* indicating that and you have successfully installed the relevant software and hardware on the computer. However, if upon clicking the HDVB icon, the following warning dialog pops up, please follow the rest of the instructions in this section. **Note**. The dialog box shown is *Figure E-10* will also appear if the GUI is launched while the board is powered down.

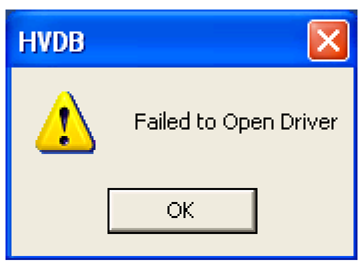


Figure E-10. HVDB Warning

5. Go to Start -> Control Panel -> Add Hardware. This will bring up the Add Hardware Wizard as shown in *Figure E-11*. Click on “Next.”

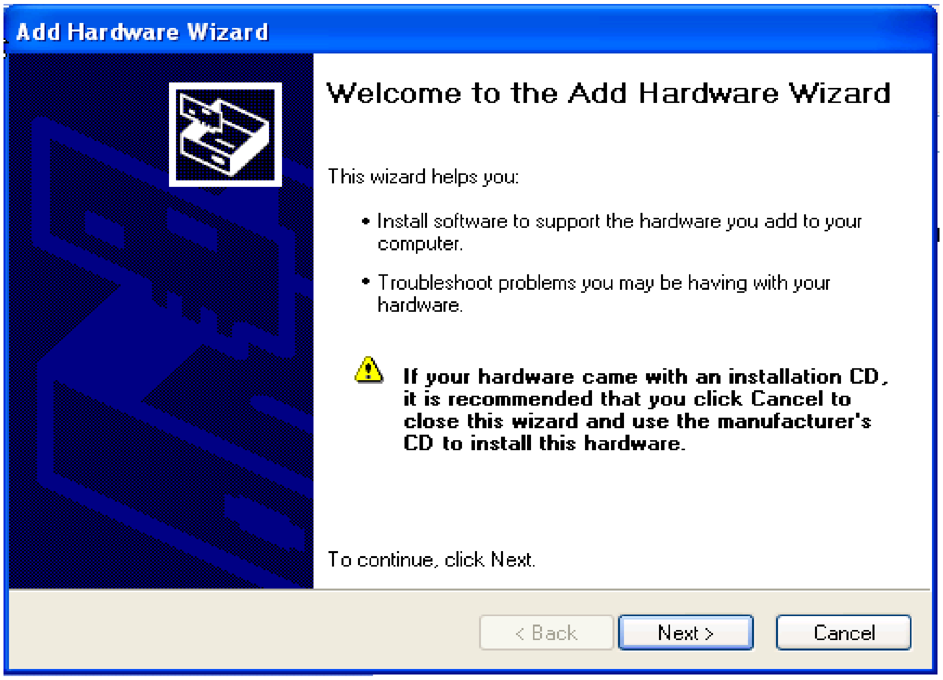


Figure E-11. Add Hardware Wizard

6. Make sure the USB cable is connected to the PC/laptop at this point. The "Yes, I have already connected the hardware" option should be checked by default. Click on "Next."

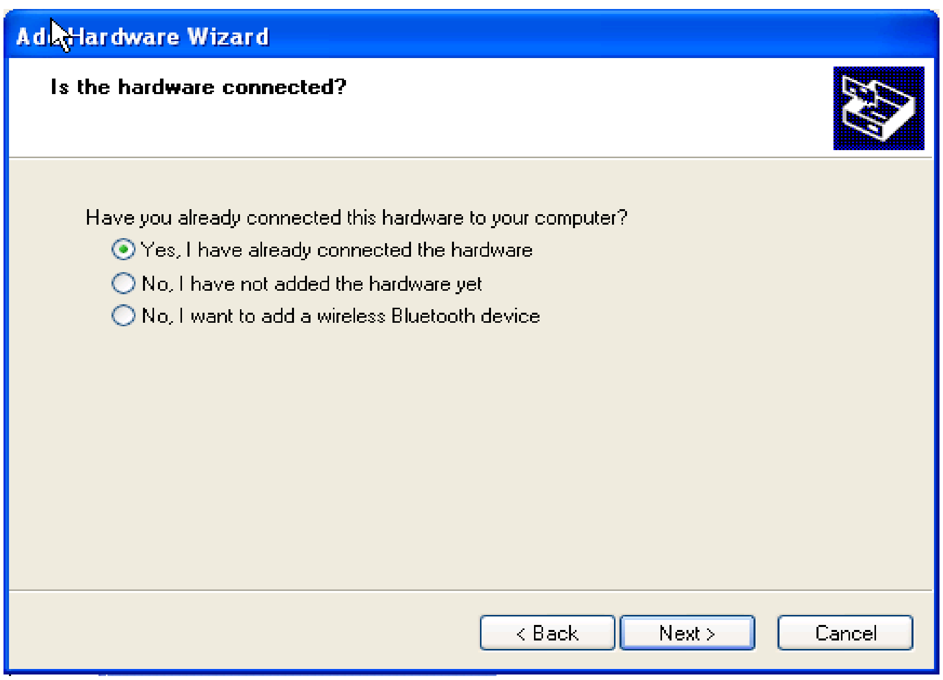


Figure E-12. Add Hardware Wizard 2

7. Select the “Cypress HOTLink II Video Demo Board” hardware already installed on the computer.

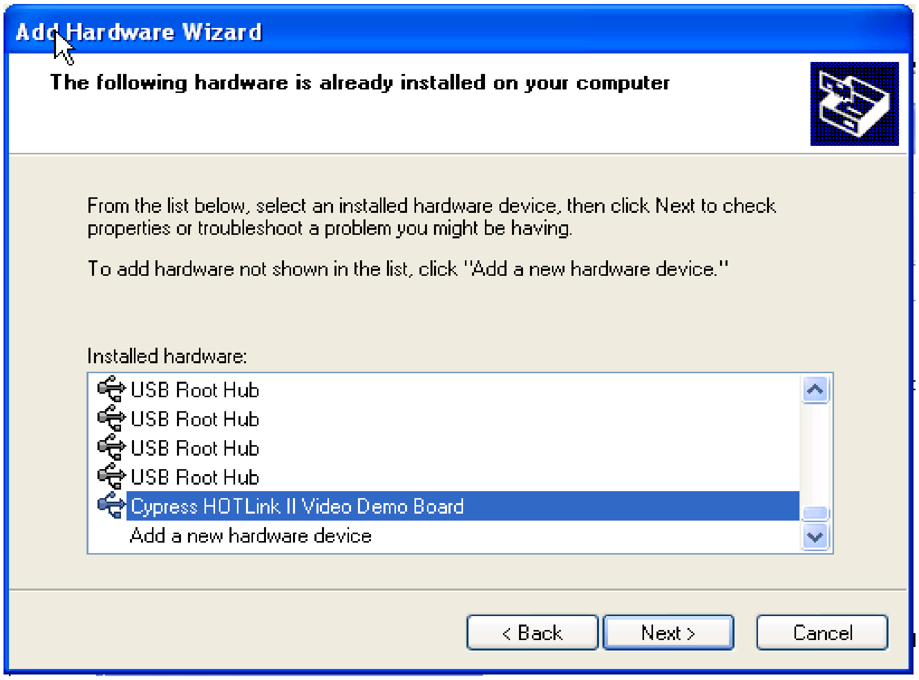


Figure E-13. Add Hardware Wizard 3

8. Click on “Finish” when the hardware is configured properly.



Figure E-14. Add Hardware Wizard 4

- The GUI looks like the following.

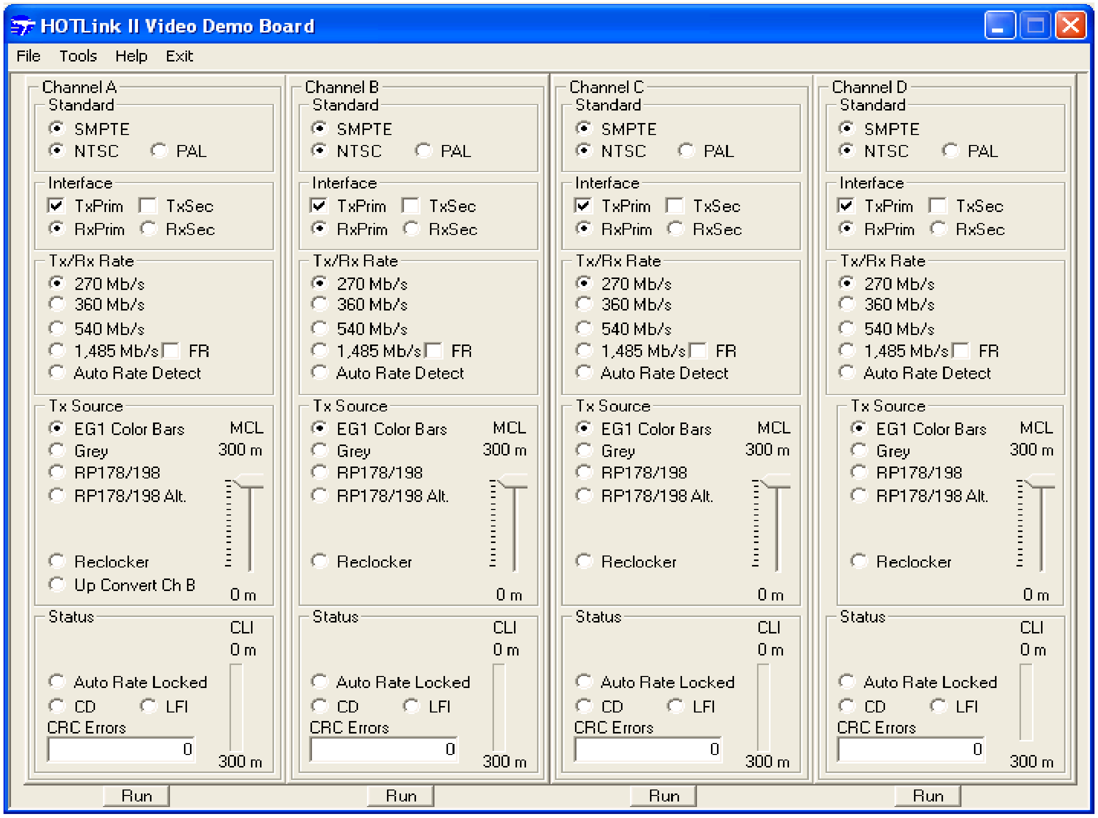


Figure E-15. HVDB Graphical User Interface

Board Configuration Instructions

Please note that the FPGAs and PSoC are preprogrammed at the factory, for testing purposes. Therefore, you should have no need to perform the following steps. They are included as a reference should you ever need to reprogram the board.

1. Double click on the HDVB icon. The GUI should appear.
2. Click on Tools ->FPGA Programming. A small dialog box should pop up as shown.

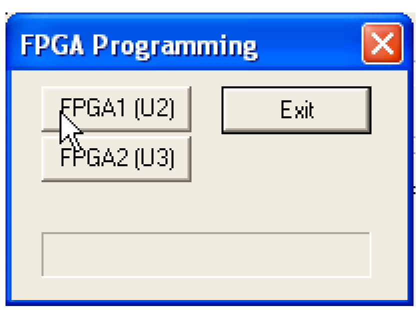


Figure E-16. GUI–FPGA Programming Dialog Box

Click on FPGA1 (U2). This will bring up a File Open dialog box. Select “Hdvb0.pof”. Click on “Open”. The dialog box will have a “percentage complete” indicator which indicates if the erasing/programming is completed. The FPGA will first be erased, then programmed. When “Programming U2 Complete” is indicated on top of the “percentage complete” bar, click on “Exit” to close the dialog box. The FPGA 1 (U2) is now configured. The series of status indications of the dialog box is shown in the following figures.

[+] Feedback

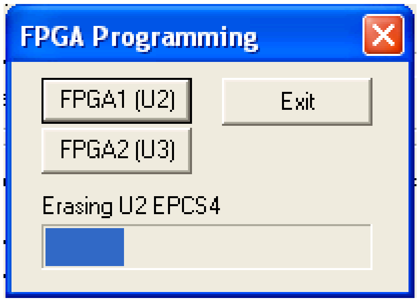


Figure E-17. FPGA Programming Dialog Box 1

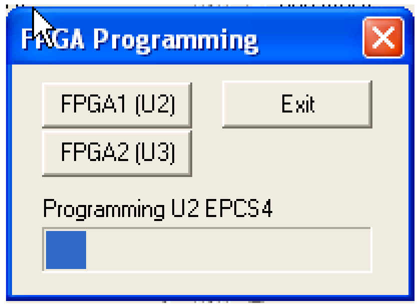


Figure E-18. FPGA Programming Dialog Box 2

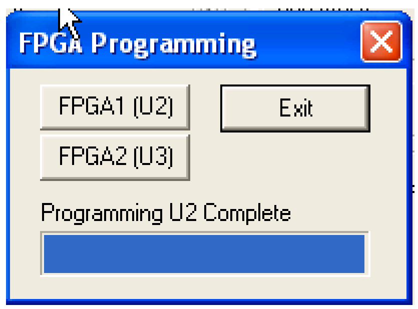


Figure E-19. FPGA Programming Dialog Box 3

Click on FPGA2 (U3). This will bring up a “File Open” dialog box. Select “Hdvb1.pof.” Click on “Open.” The FPGA is configured the same way as in (1).

3. Click on Tools->PSoC Programming. A small dialog should pop up as shown. Click on “Program PSoC.” This will bring up a File Open dialog box. Select “Hdvb.hex.” Click on “Open.” PSoC is now configured.

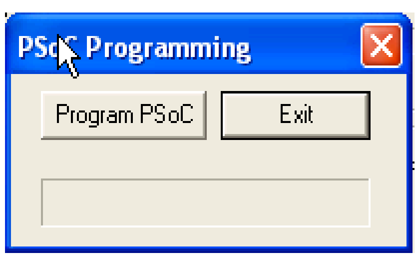


Figure E-20. GUI PSoC Programming Dialog Box

Setting Configurations

Once the user has configured the desired settings on the GUI, the settings selected can be saved to a file for future retrieval. Similarly, a user can retrieve a saved setting.

- To save a current setting, click on File -> Save Settings, the “Save As” dialog box will prompt the user to enter a valid file name and the setting for the GUI is saved as a configuration file with an “.ini” file extension. Click on “Save” to save the file. See *Figure E-21*.
- To load a saved setting, click on File -> Load Settings, the “Open” dialog box will prompt the user to select a valid existing configuration file. Click on “Open” to open the file. The GUI settings should be loaded with the new setting.

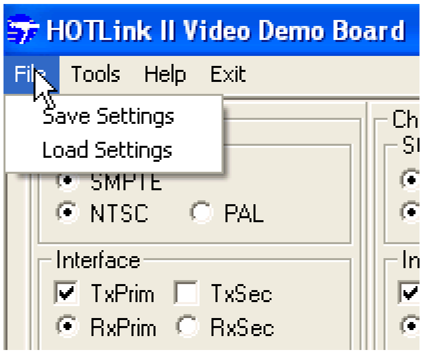


Figure E-21. GUI–Save/Load Settings

Appendix F: Configuring the HOTLink II CYV15G0404DXB Video Demo Board for SD-SDI to HD-SDI Upconversion

[+] Feedback

Overview

This appendix discusses the necessary modifications that need to be made to the CYV15G0404DXB video demo board, in order for it to be able to perform upconversion. The upconversion function described in this appendix is for functional verification only. Due to design constraints, the measured jitter will be higher than normal. If you have any questions about this feature please contact Cypress's Application Engineers.

Upconversion

Upconversion is the process of manipulating SD video data to produce an HD version of the same video. An SD signal is scaled to the desired number of horizontal lines per frame, as well as the appropriate number of pixels per line. The resulting HD signal can be used to drive a high-resolution projector or monitor.

Upconversion may be used in broadcast situations where SD video masters are provided to stations that wish to broadcast in HD. For example, if a show is produced in 480 line interlaced and is provided to a station that wishes to broadcast in 1080 line interlaced, an upconversion would be required. Upconversion can also be used when programming is broadcast in HD, but advertisements are in SD format. An upconversion will enable the transmission of the advertisements in HD format.

In the CYV15G0404DXB video evaluation board, incoming SDI data that needs to be upconverted is input to the channel B receiver of the HOTLink II device. The deserialized video data is processed by the FPGA where it is upconverted and transmitted through the channel A transmitter of the HOTLink II device. The upconversion process is comprised of two primary components: scaling of the video from 720 by 483 to 1440 by 1035 and conversion of the clock frequency from 27 MHz to 74.25/1.001 MHz. *Figure F-1* shows the block diagram for upconversion through the CYV15G0404DXB video demo board.

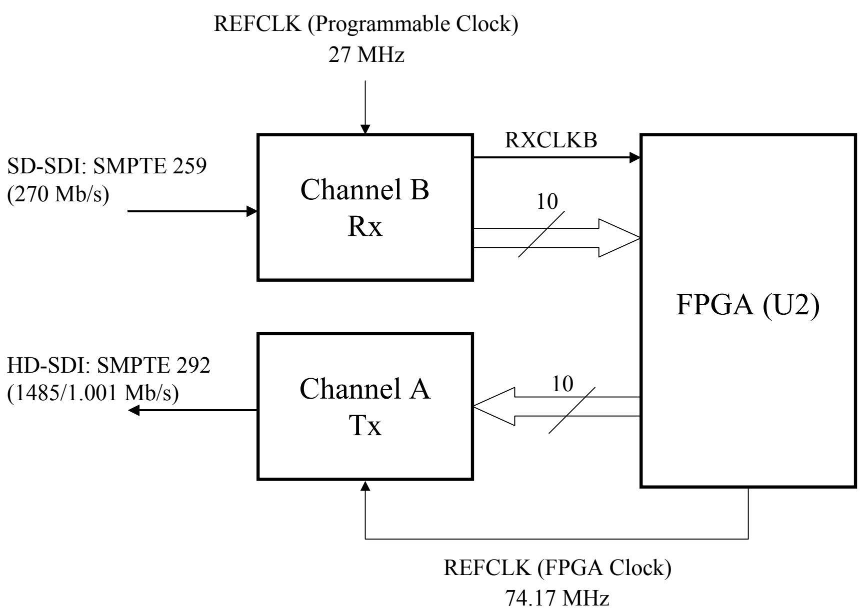


Figure F-1. SD-SDI to HD-SDI Upconversion Block Diagram

Video Scaling

To perform the video scaling, the incoming SDI data is stored and scaled in up to seven line buffers. For each seven lines of SDI data input, the first six lines are repeated twice, and the seventh line is repeated three times. The result is 15 lines of HD-SDI data for each seven lines of SDI data in. The original SD-SDI image of 720 by 483 is converted to an HD-SDI image 1440 (720*2) by 1035 (483*15/7). This changes the aspect ratio of 4:3 (1.333:1) to [4*15]:[3*14] (1.429:1). The resulting image is stretched vertically by about 7%, but matches the average line and frame rates for incoming and outgoing data. In order to generate HD-SDI line data, each pixel sample pair is repeated twice as follows.

$C_{Rn}Y_nC_{Bn}Yn+1$ -> $C_{Rn}Y_{2n}C_{Bn}Y_{n+1}R_{n+1}Y_{n+1}C_{Bn+1}Y_{n+1}$

[+] Feedback

Clock Rate Conversion

As part of the upconversion process, the incoming SDI clock rate (27 MHz) must be converted to HD-SDI (half rate at 74.25/1.001 MHz). To achieve this, both PLLs in FPGA(U2) are connected in series to get the correct frequency for transmitting. The 27-MHz clock rate from RXCLKB+ is passed through FPGA(U2), where the first PLL multiplies RXCLKB+ by 25/13, while the second PLL multiplies the result by 10/7. This produces the desired half rate frequency of 74.17 MHz (74.25/1.001 MHz), which is sent to the reference clock for channel A (REFCLKA).

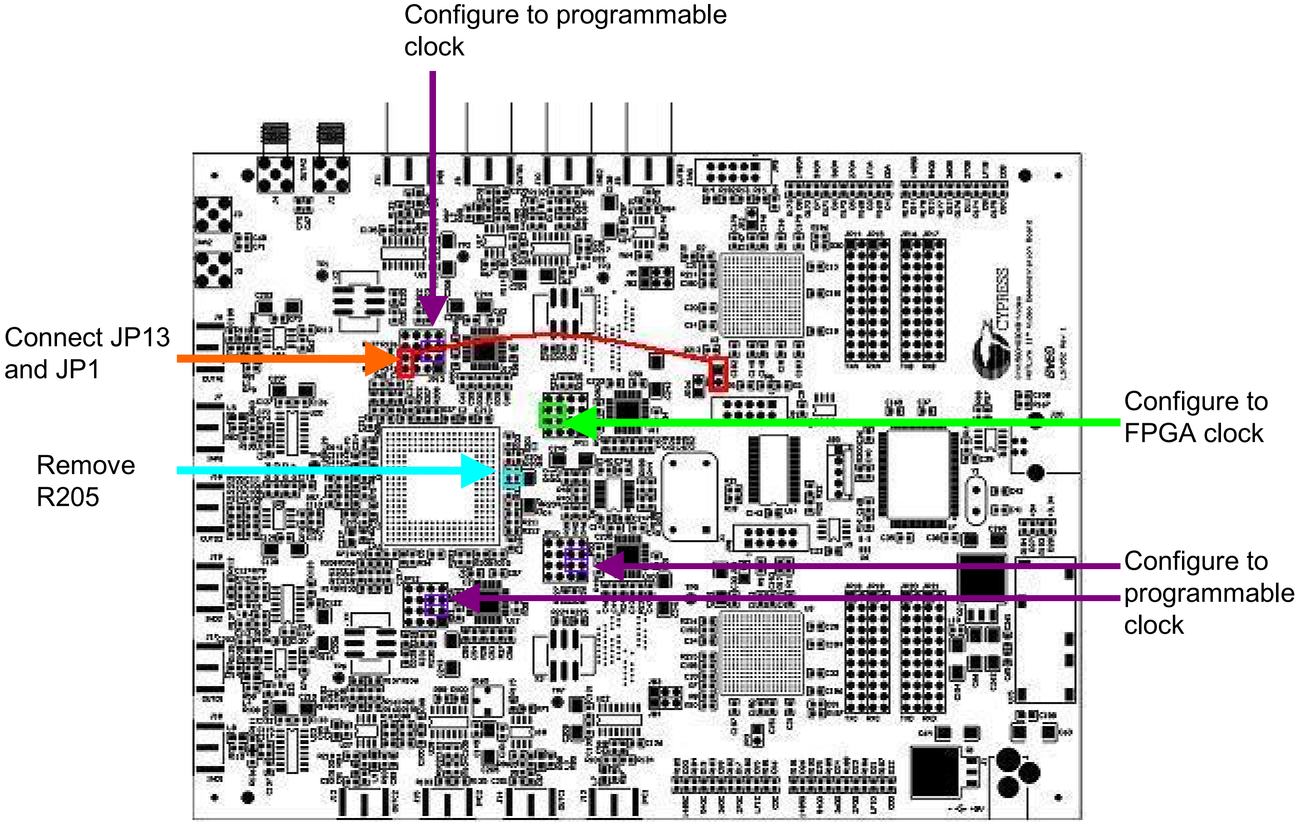


Figure F-2. Upconversion Board Modifications

Board Modification

The following describes the board modifications required to achieve the clock rate conversion.

1. Connect JP13 (FCLKB+) and JP1 (RXCLKA+) as indicated in *Figure F-2*. Refer to *Figure F-3* for location of the ground pins.

   RXCLKB+ is connected to the first PLL in FPGA(U2), while the output of the PLL is internally connected to FCLKB+. By connecting JP13 and JP1 as indicated, the output of the first PLL (FCLKB+ output pin) is sent to the input of the second PLL (RXCLKA+ input pin) in FPGA(U2).

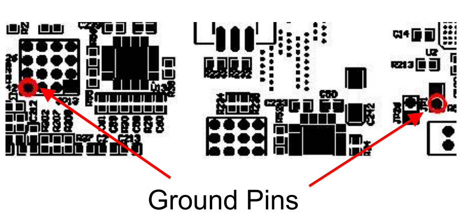


Figure F-3. Ground Pin Location

2.Remove resistor R205.

The RXCLKA+ pin on FPGA(U2) is connected to the input of the second PLL in FPGA(U2). However, the RXCLKA+ output pin of the CYV15G0404DXB chip is connected to the RXCLKA+ input pin of FPGA(U2). The removal of resistor R205 breaks this connection and allows FCLKB to be routed through the second PLL.

3. .Configure clocking options to FPGA clock option for Channel A (JP11).

This sets the reference clock for Channel A (REFCLKA) to the FPGA clock (FCLKA). Refer to theCYV15G0404DXB User's Guide for further information on clocking options.

4. Configure clocking options to programmable clock option for Channels B, C, D.

The block diagram for the resulting clock circuit is shown in *Figure F-4*.

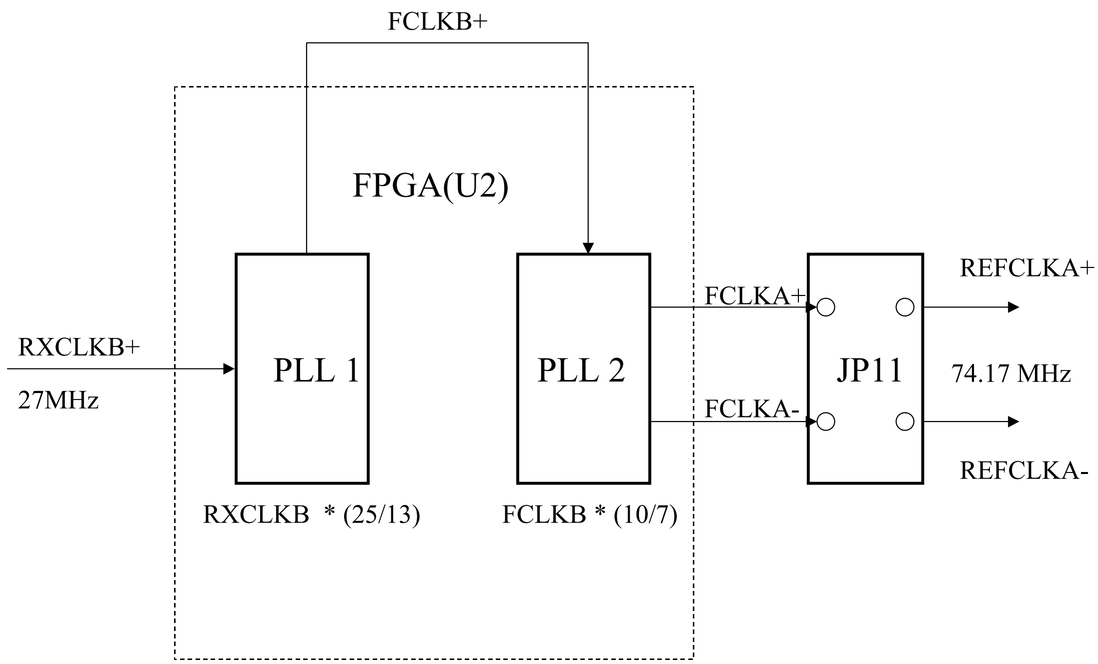


Figure F-4. Upconversion Clock Circuit

Test Procedure

Transmission of the SD-SDI signal may be generated on either channel C or channel D. This application note will describe the connections and settings required for upconverting an SD-SDI signal transmitted on channel C.

Board Connections

1. Apply power to the board and connect the USB cable between the board and the computer.
2. Connect output OUTC1 to input INB1 using a BNC cable.
3. Connect output OUTA1 to the WFM700 using a BNC cable.

Figure F-5 shows the required board connections.

[+] Feedback

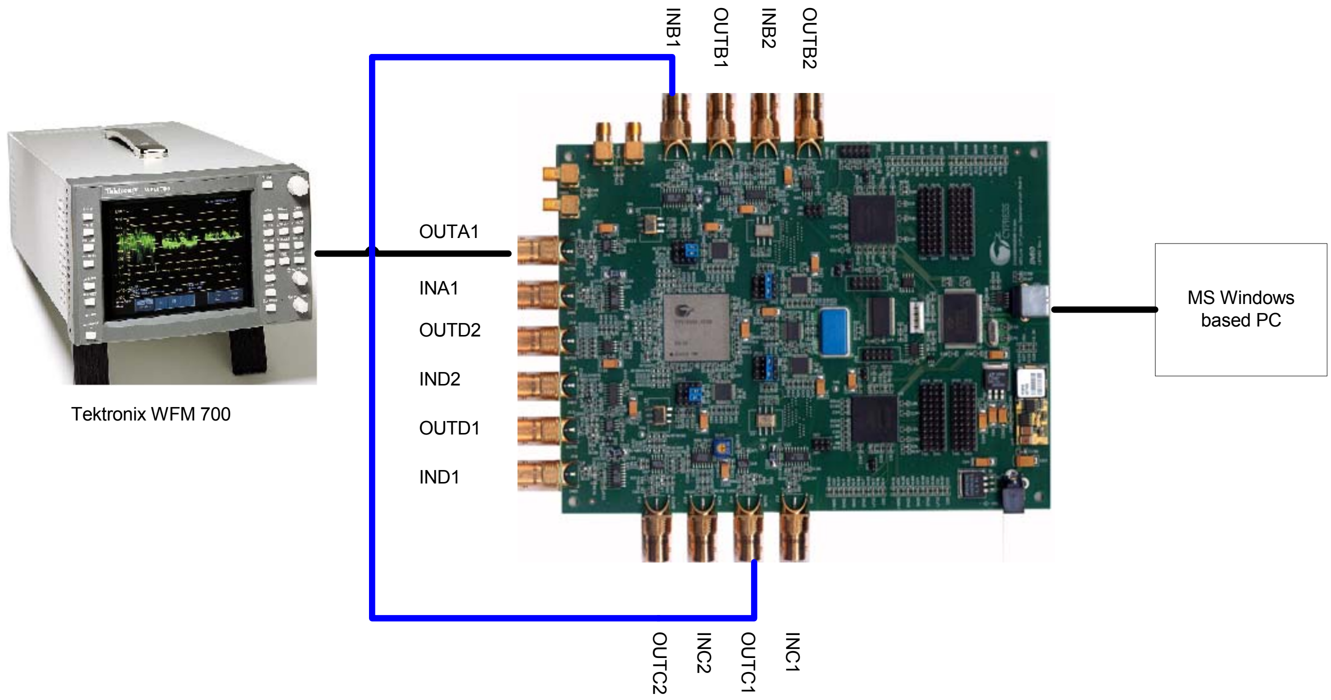


Figure F-5. Upconversion Test Connections

GUI Configuration

Configuration of the CYV15G0404DXB GUI is comprised of the following steps. The typical settings are shown in *Figure F-6*.

1. Enable an SD-SDI/SMPTE 259M-C signal by selecting 270 Mb/s in the Tx/Rx Rate Box of the GUI.
2. Select “Up Convert Ch B” on channel A
3. Run channels A, B, and C

[+] Feedback

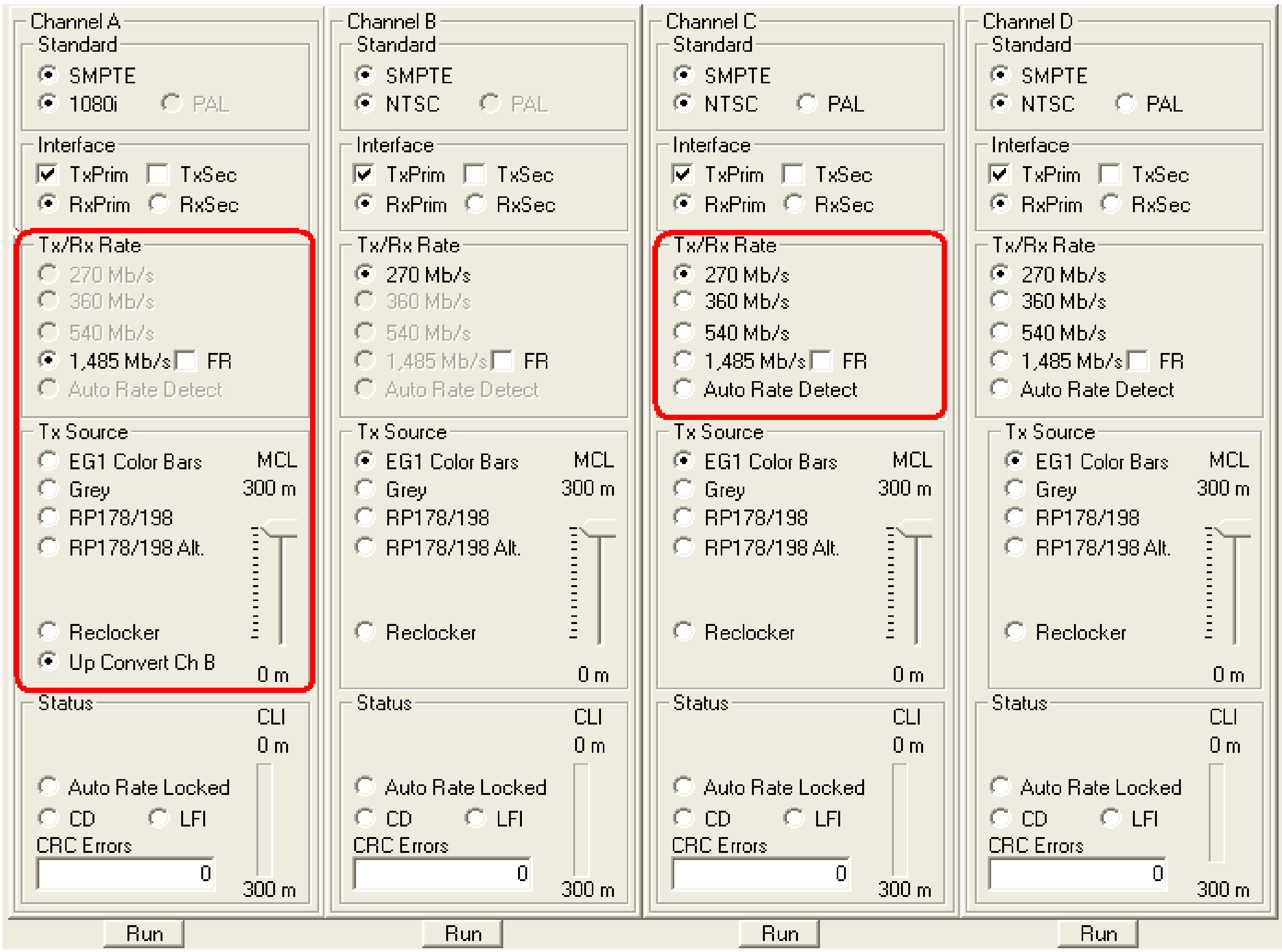


Figure F-6. Upconversion GUI Settings

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Results

The output of the upconverted signal may be verified by monitoring the output signal on any HD-SDI waveform monitor (example Tektronix WFM 700). *Figure F-7* and *Figure F-8* show the output for an SD-SDI, HD-HDI, and upconverted HD-SDI signal respectively.



Figure F-7. SD-SDI Video Picture

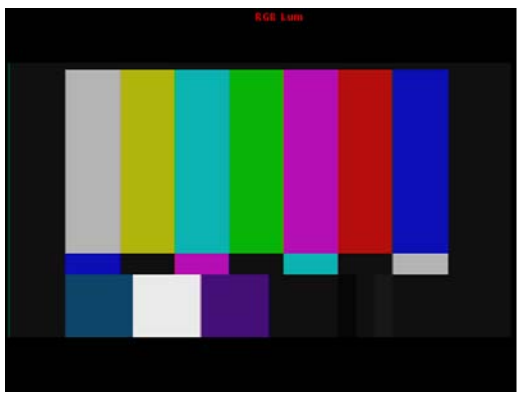


Figure F-8. Upconverted HD-SDI Video Picture

Unused active video samples in active outgoing video lines are set to black. This will result in the black bars at the sides of the video image in *Figure F-8*. Some active video lines at the top and bottom of the HD-SDI output are not used, and result in the black bars above and below the image.

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